The FlashCam Project

A fully digital camera for future Cherenkov telescopes

- FADC-based system
- Digital FADC/FPGA trigger
- GBit Ethernet front-end readout

ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich

University of Zurich[UZH]

AGH

AIT

ecap

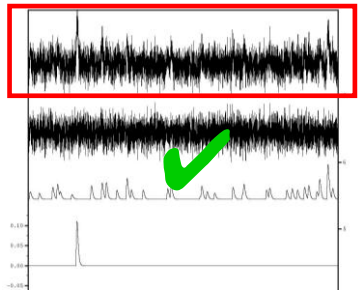
University of Leicester

Speaker: Arno Gadola, Uni. Zurich

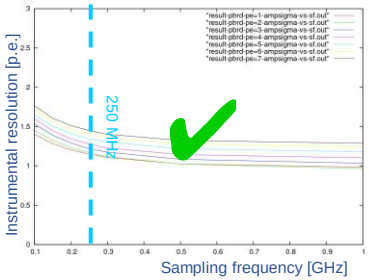
FlashCam: Extensive Simulations …

Simulations and measurements have shown: 250 MS/s digitization highly competitive

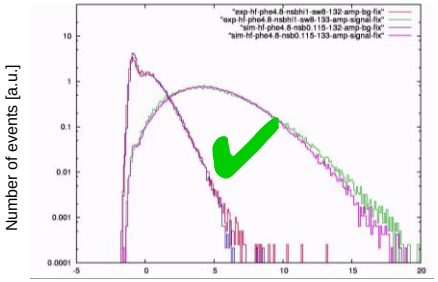
MC WP is starting to implement 250 MS/s digitization for cross-check



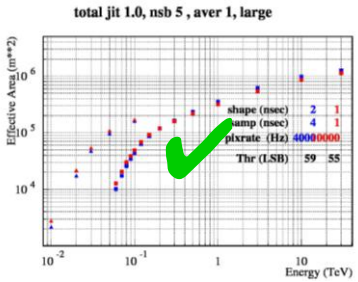
Simulation of 2GS/s and 250 MS/s digitization



Resolution above 250 MS/s approx. constant (simulation)



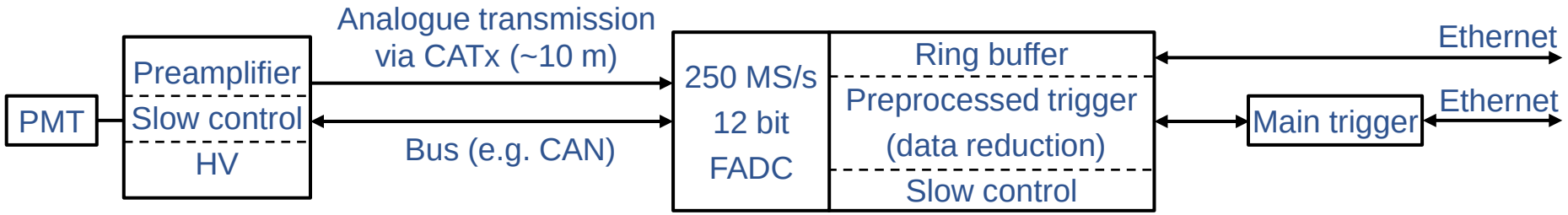
Comparison and confirmation of resolution at 2GS/s and 250 MS/s with measurements



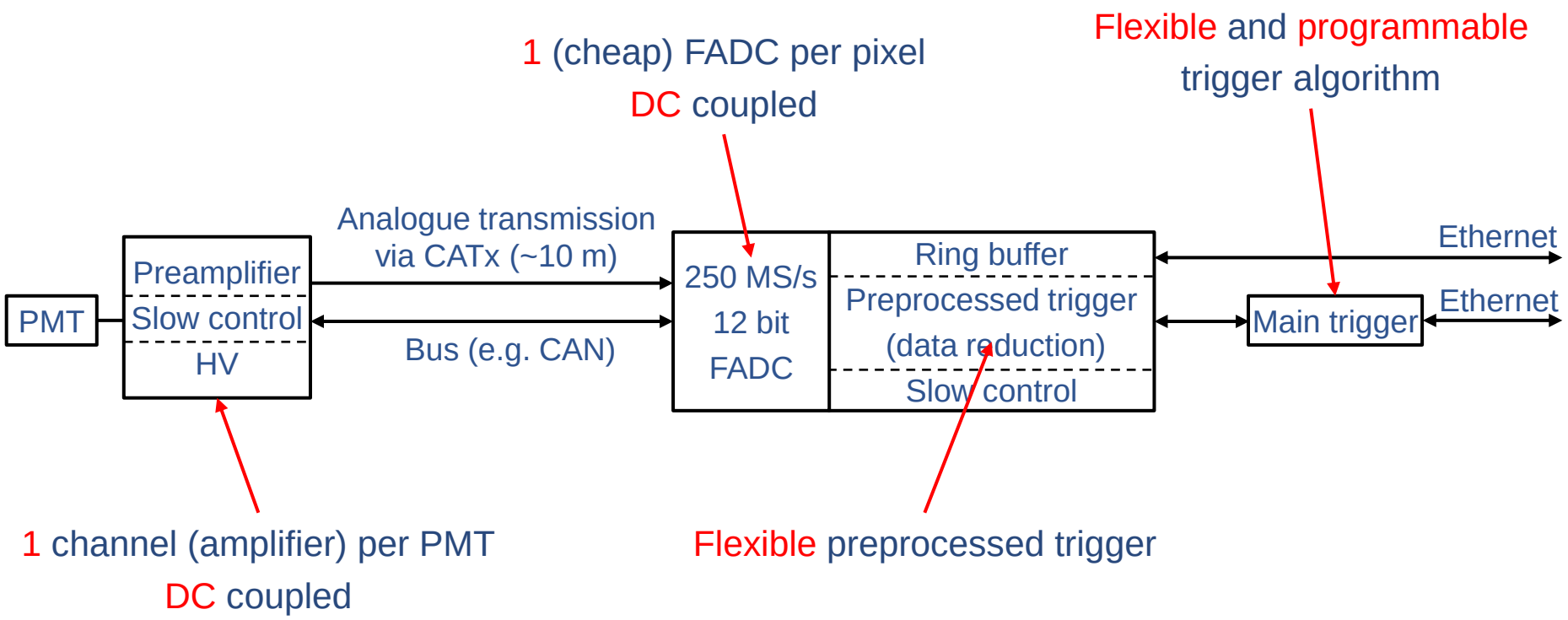
Trigger topology-, time jitter-, NSB- and other studies

MPIK + Uni Zurich

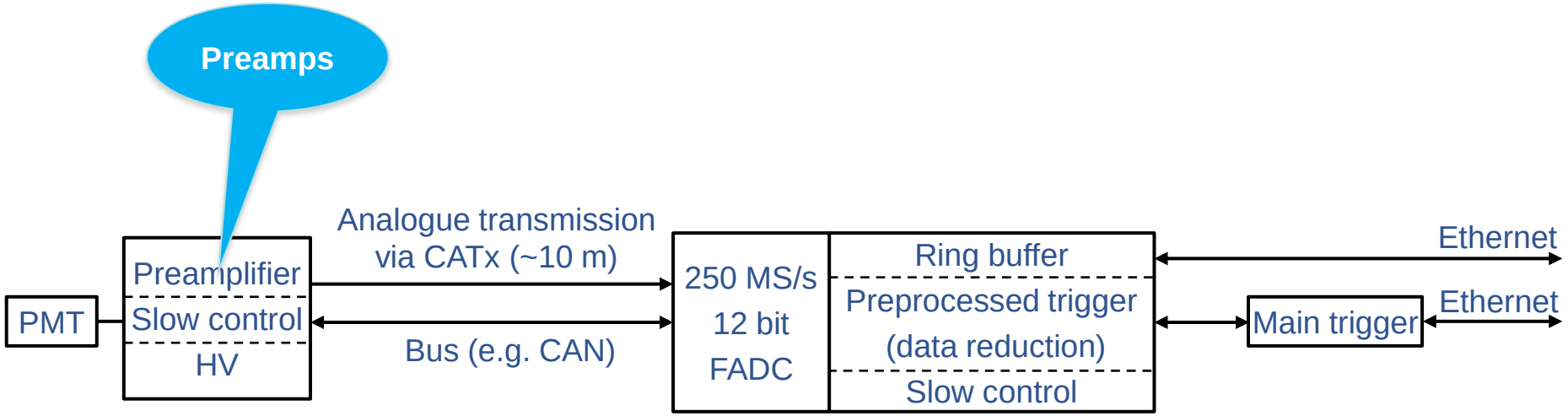
FADC-based front-end: Baseline topology



FADC-based front-end: Features



Camera Architecture



Preamplifier

Linear preamplifier

- two channel
- different amplification to increase dynamic range
- 12-bit FADCs per P

Nonlinear preamplifier

- **Only one amplifier** per PMT needed
- only one (12-bit) FADC per PMT
- Three approaches:
  - op-amp in saturation
  - transistor in saturation
  - nonlinearity of diode

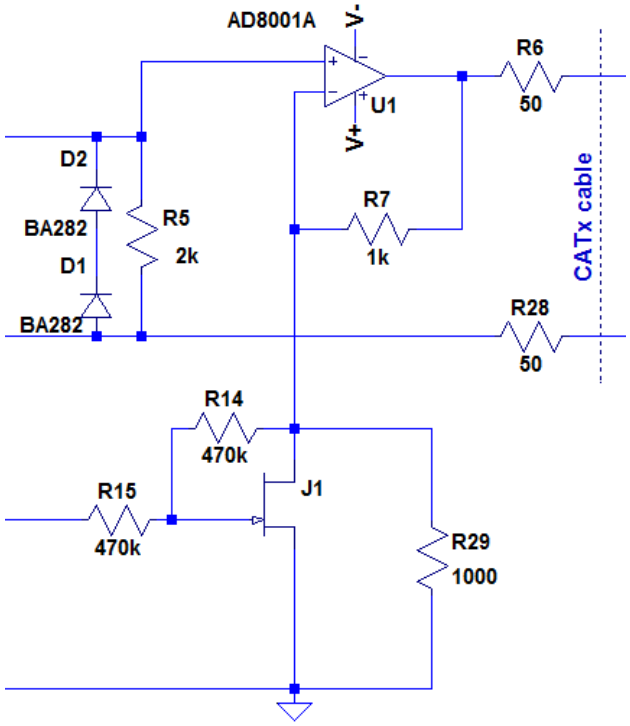
Cracow + Uni Zurich + MPIK

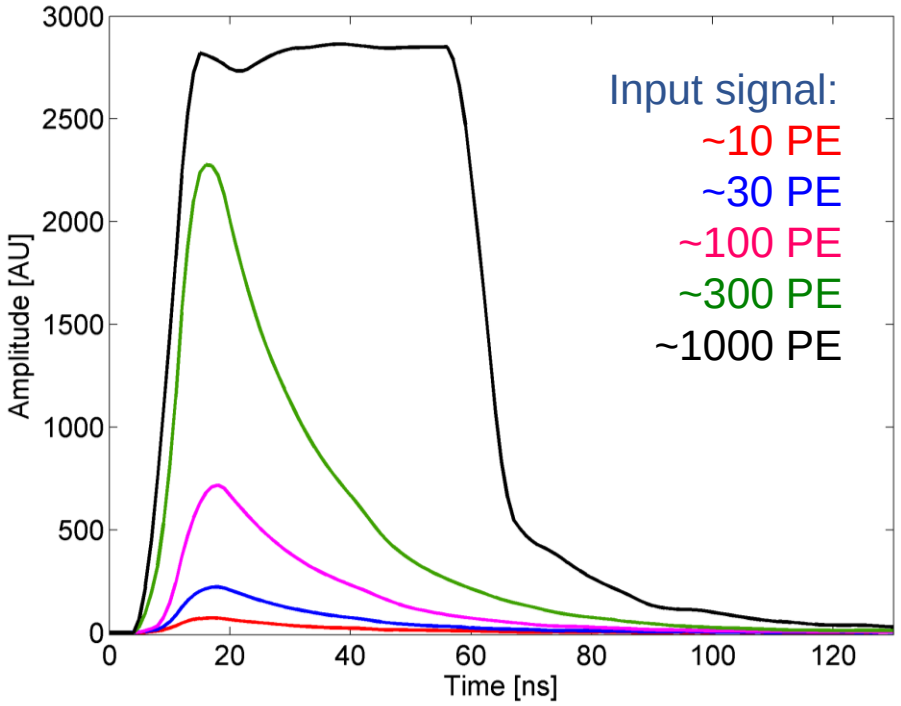
Saturation preamplifier: baseline

- ~0.1 to 3000 PE dynamic range
- Saturation starts at about 200 PE (~ 8 LSB / PE)
- Saturation is a documented feature

- Working on variable gain
- Baseline solution for parallel FADC demo board

MPIK + Uni Zurich



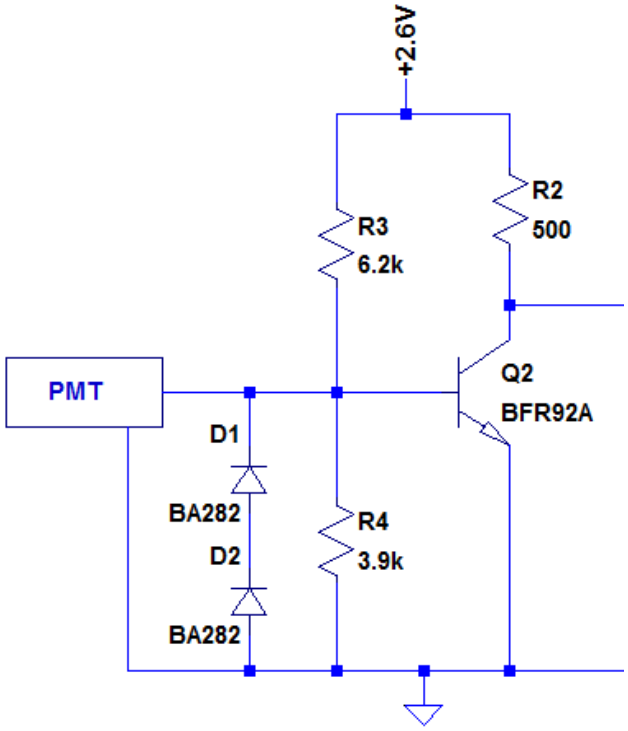


Measurement of one event (fs = 250 MS/s, interpolated and smoothed)

Transistor preamplifier: option I

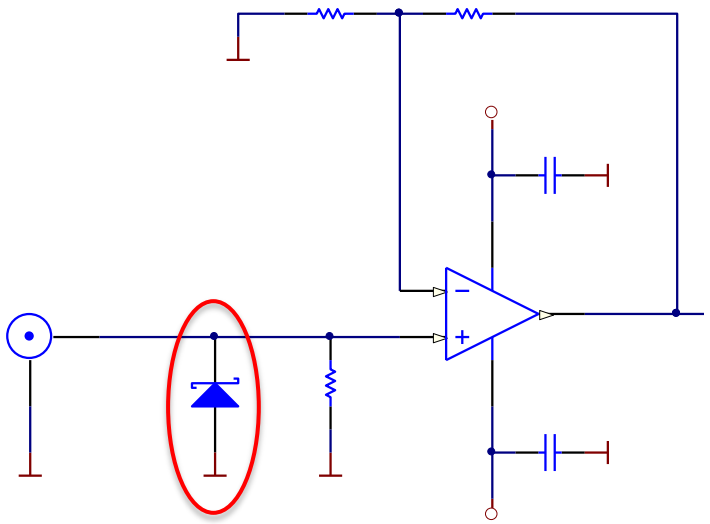
MPIK + Uni Zurich

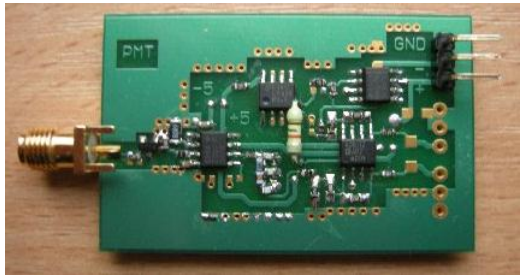
- ~0.1 to 3000 PE dynamic range
- Saturation starts at about 200 PE
  (adjustable through power supply voltage)
- First measurements done
- Cheap and low power (~15 mW/pixel)



„Diode“ preamplifier: option II

- Nonlinear preamp simulated and tested in the lab
- More development needed





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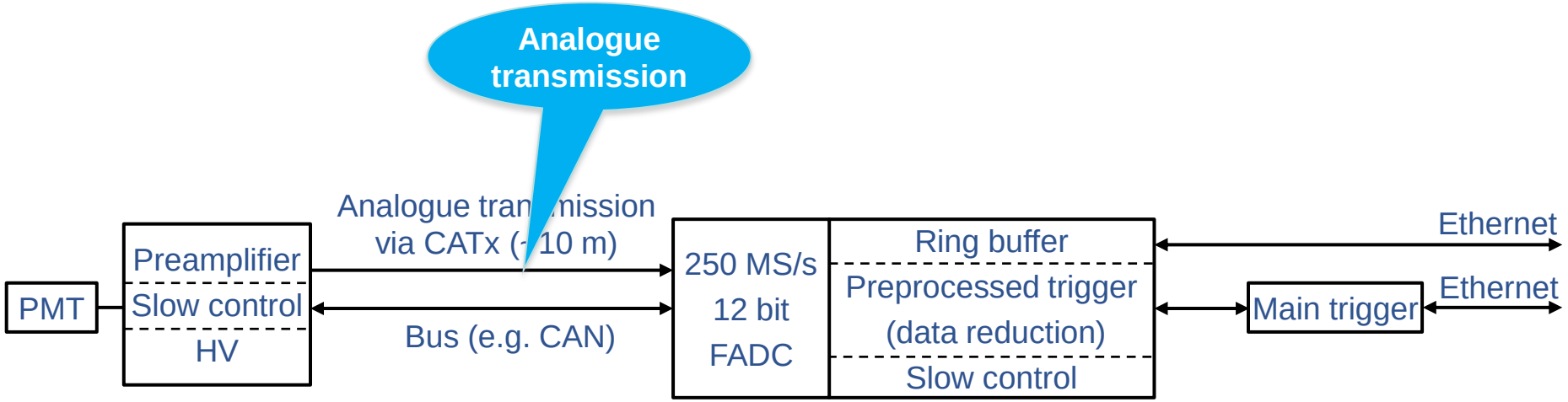
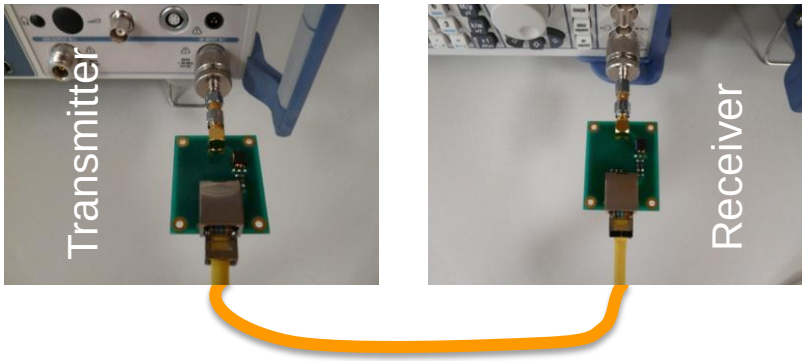
Camera Architecture



CAT 5 for Analogue Signal Transmission

CATx cable for analogue signal transmission



- Signal transmission over CAT5/6 cable
- Test signal up to 125 MHz sine wave
- Attenuation 0.4 dB / m
- Tested with cable lengths up to 10 m
- 4 pixel signals per CAT5/6 cable

✔

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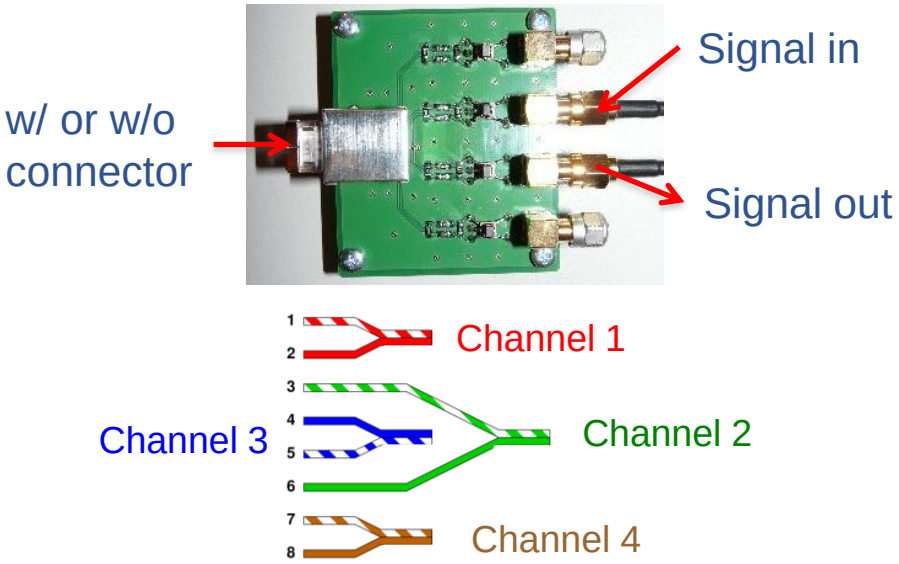
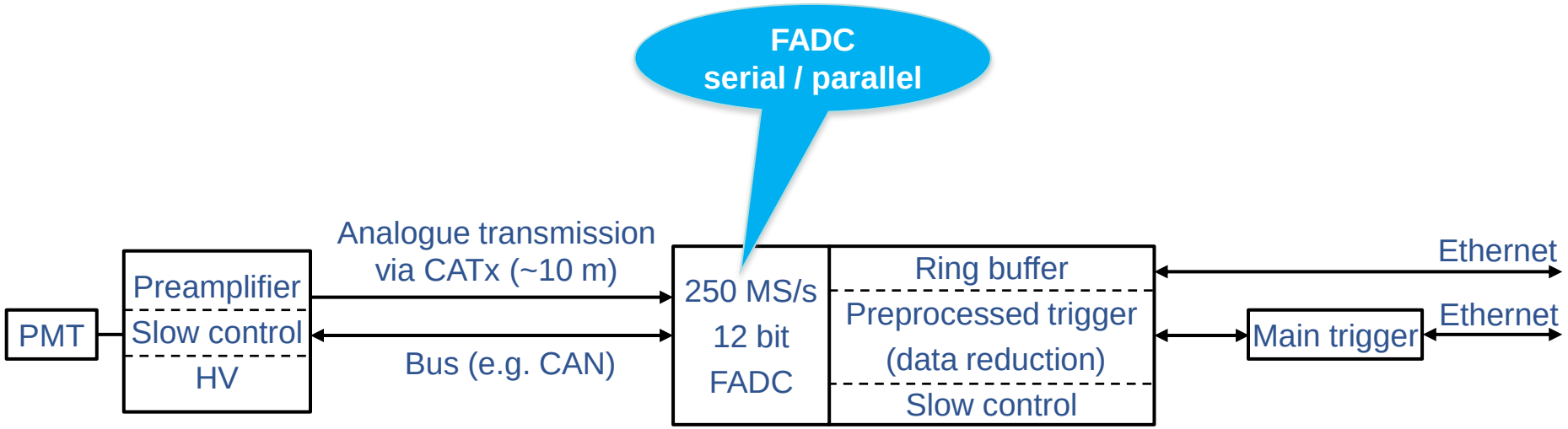
CATx cable and connector crosstalk



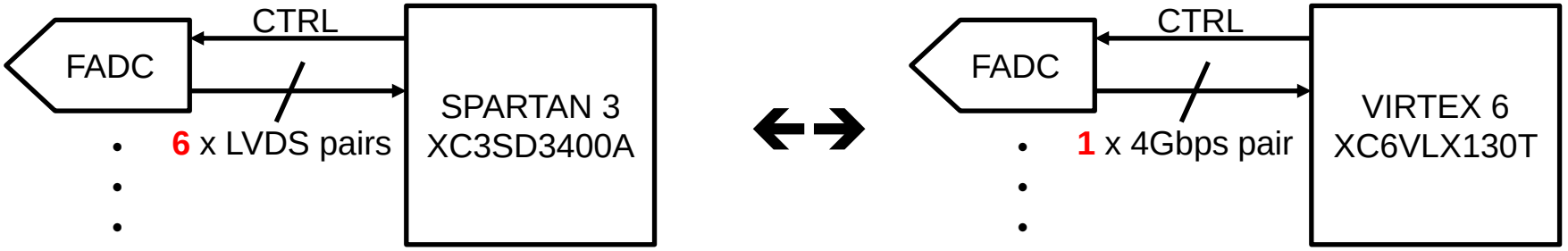
- CAT5 connectors tested
- Worst crosstalk between channel **2** and **3**
- Introduced mainly by the connector
- CAT6 and CAT6a will be tested soon

- Measured crosstalk over whole chain (preamp to FADC): 1% worst case, 0.5% typical

Camera Architecture



Parallel vs. Serial FADC to FPGA Data Transmission



Parallel FADC interface

- Pin-intensive interface to FADC
- Cheap FPGA

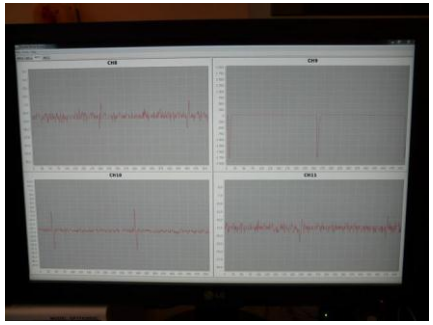
Serial FADC interface

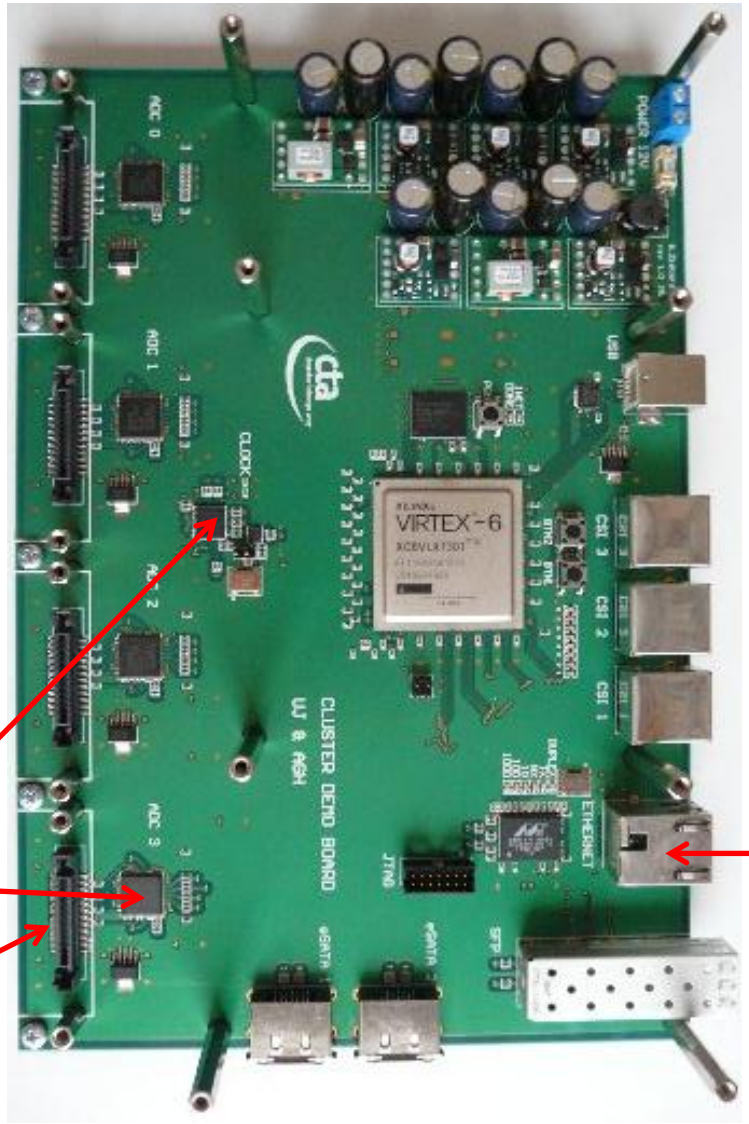
- Pin-economical interface to FADC
- Expensive FPGA

Serial FADC Demo Board

- 16 serial FADC channels
- 1Gb Ethernet readout
- Bit error measurements with internal FADC pseudorandom binary sequence generator
  ⇨ no errors during 1 h @ 64 Gb/s
- JAVA PC application

⇨ All sub-circuits tested and ready for measurements





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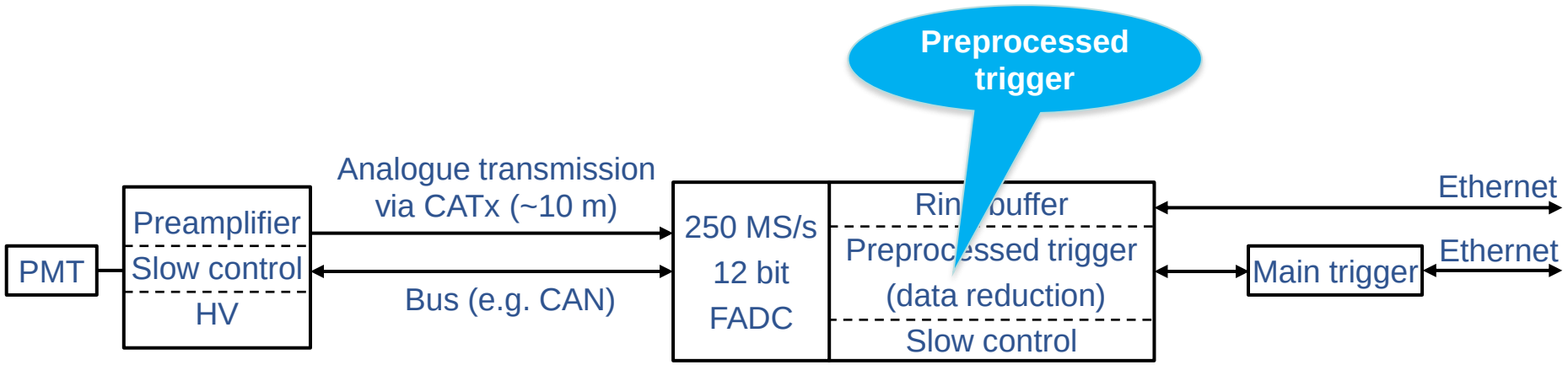
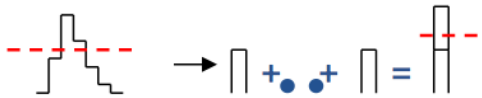
Camera Architecture

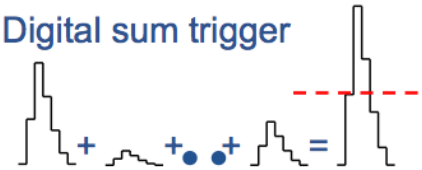


Preprocessed Trigger FPGA Layout

a) Digital majority / threshold
(w/ or w/o neighbor)



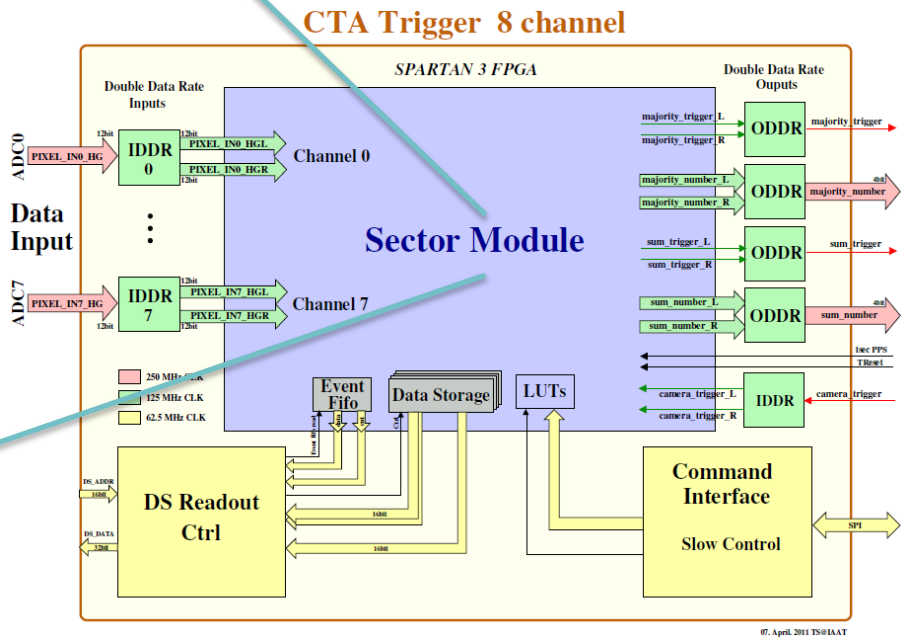
b) Digital sum trigger



c) Sum of clipped signals trigger

And other algorithms
(open to future ideas)

- Data reduction by software ⇨ flexible 'pre'-trigger
- Clipping can be switched on to suppress impact of after-pulsing
- First results have shown that FPGA meets the speed requirements
- Fine tuning of algorithm(s) ongoing
- Waiting for real hardware for implementation



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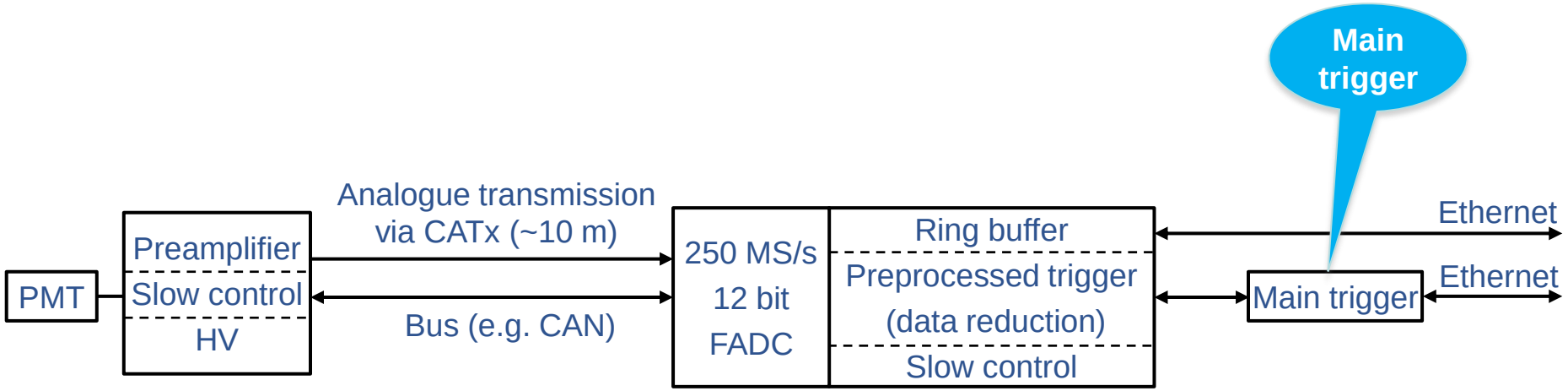
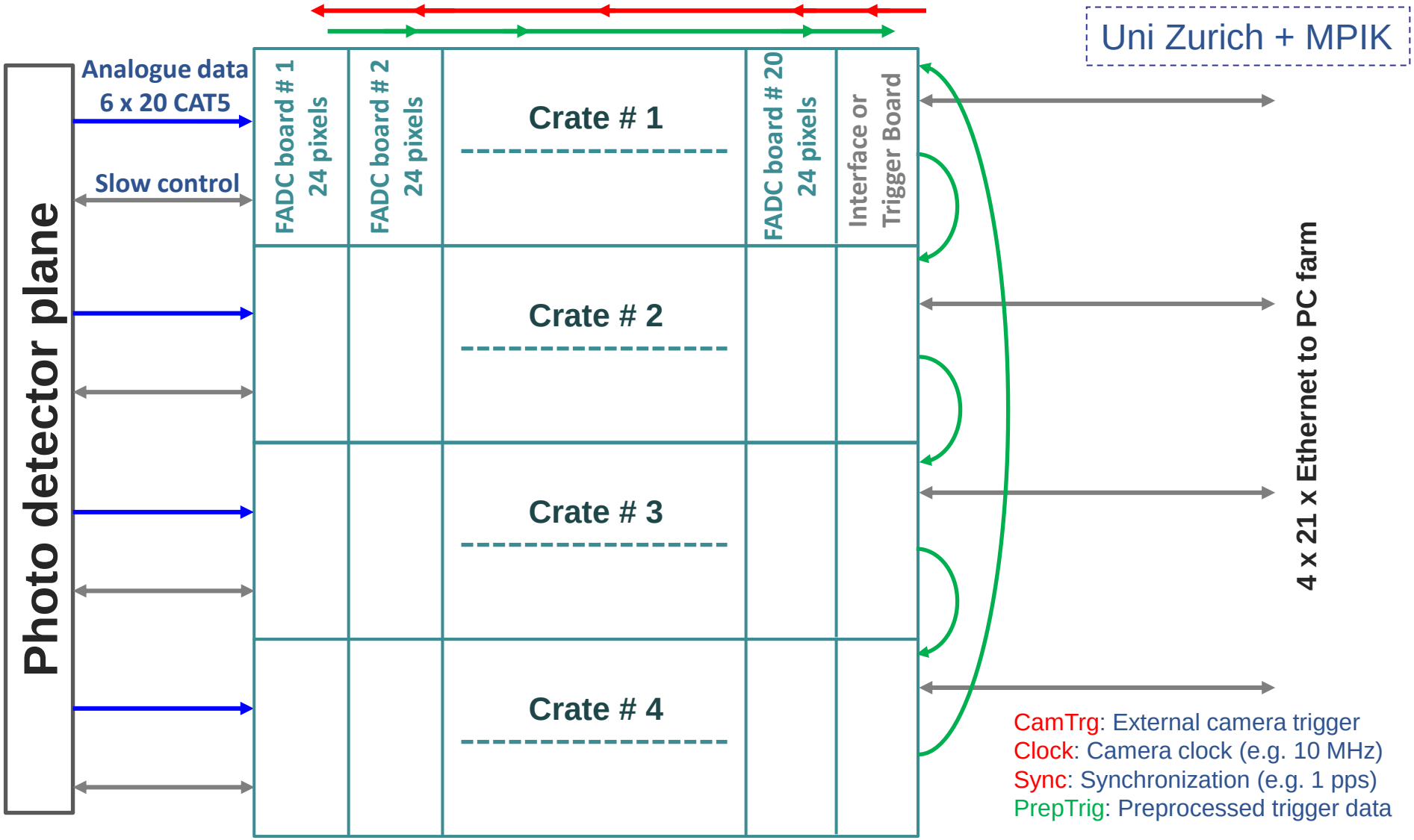
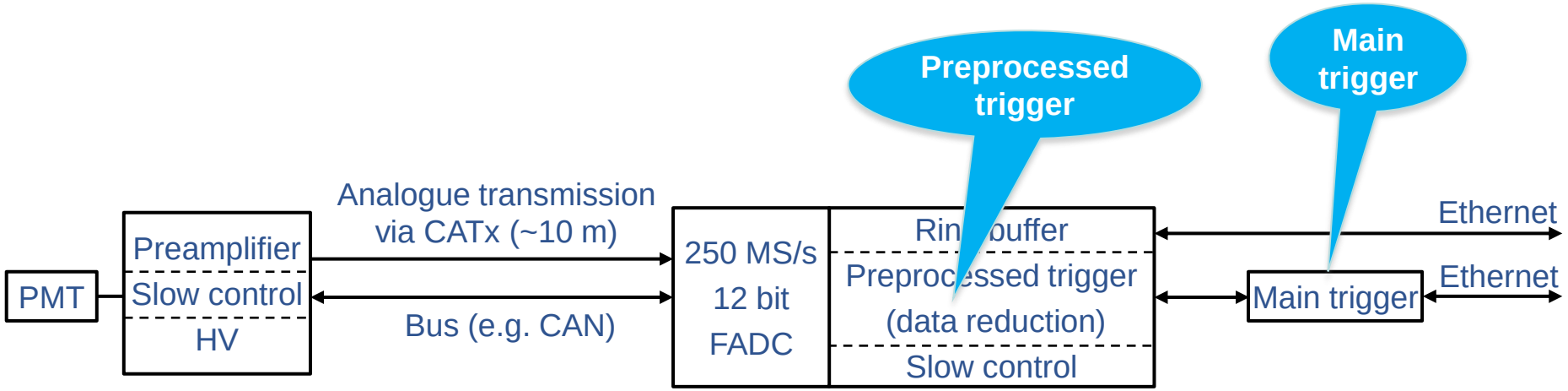
Camera Architecture



Trigger Distribution



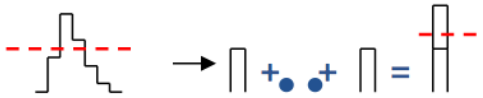
Camera Architecture



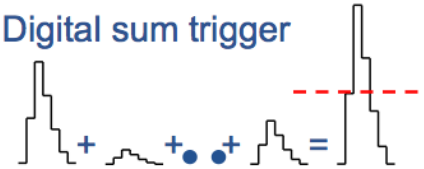
Trigger Pattern Optimization: Simulations

From low-level trigger patterns …

a) Digital majority / threshold
(w/ or w/o neighbor)



b) Digital sum trigger

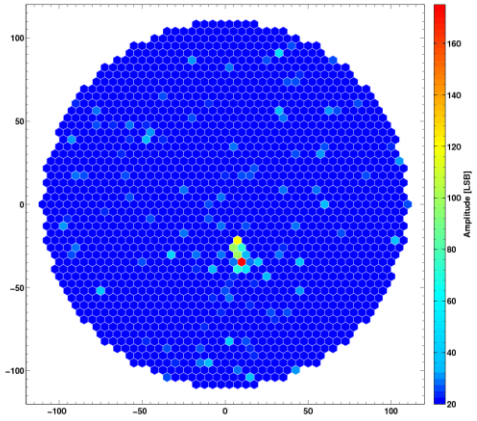


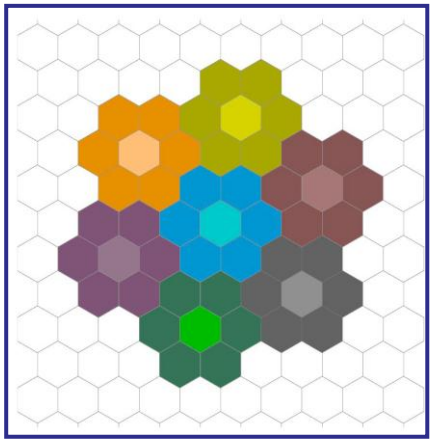
c) Sum of clipped signals trigger

And other algorithms (open to future ideas)

… to higher-level pattern recognition

300 GeV shower + 100 MHz NSB





E.g.: 7 pixel patch trigger:

- Individual patch sum
- Sum of adjacent pairs
- Sum of adjacent triplets
- Other trigger topologies

⇨ highly flexible and programmable trigger

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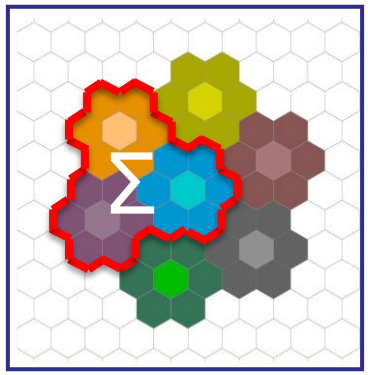
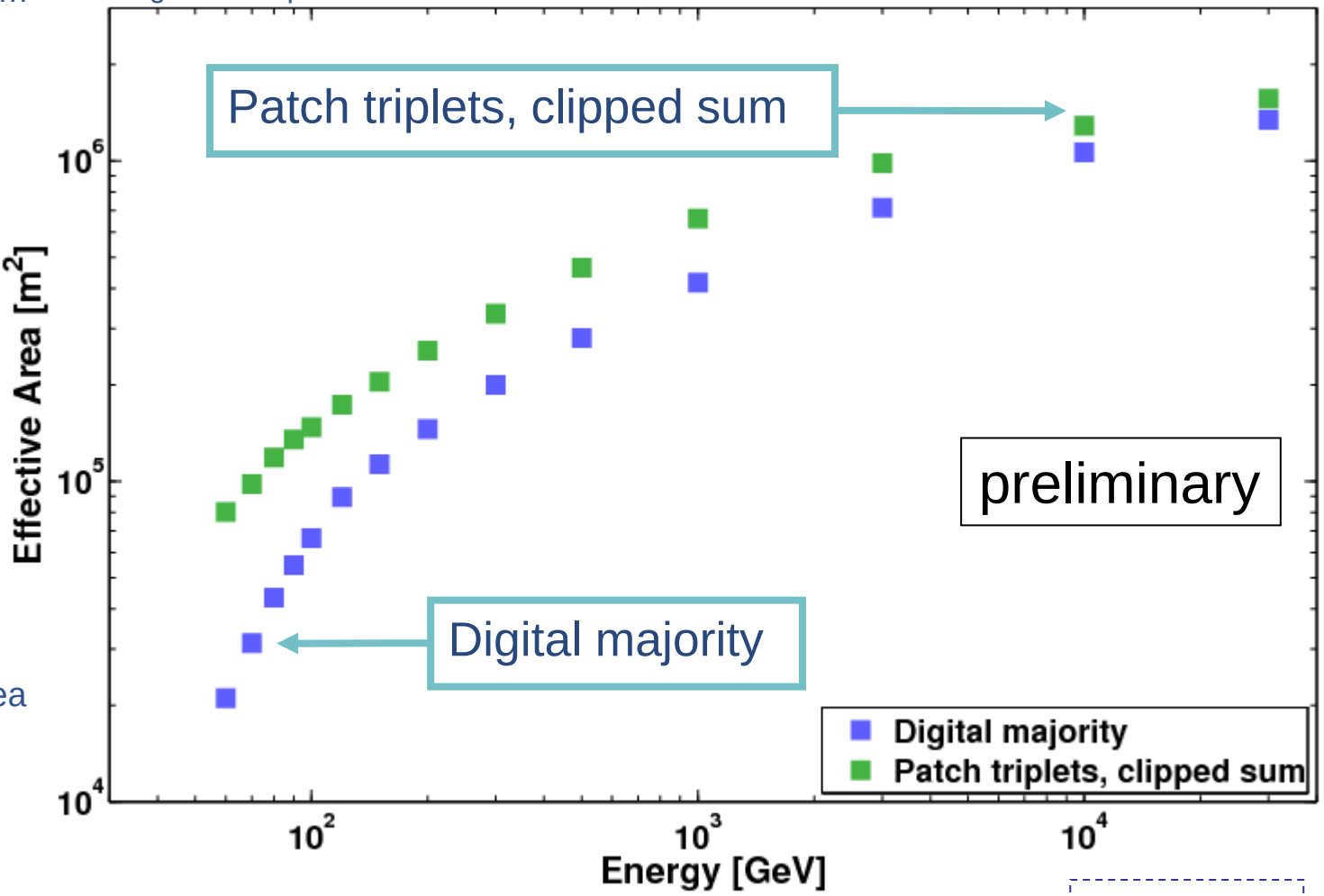
Flexible Programmable Trigger

Patch triplets, clipped sum



E.g. 100 GeV shower:
~2.3 higher effective area

Single telescope



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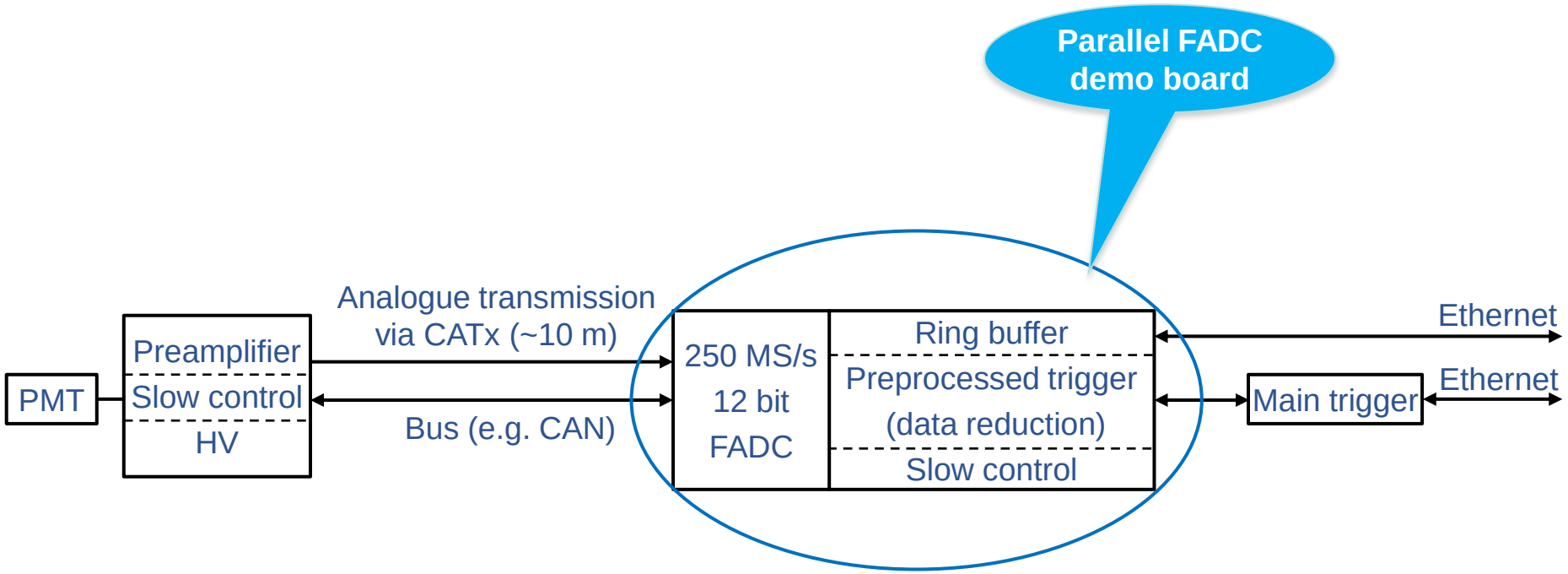
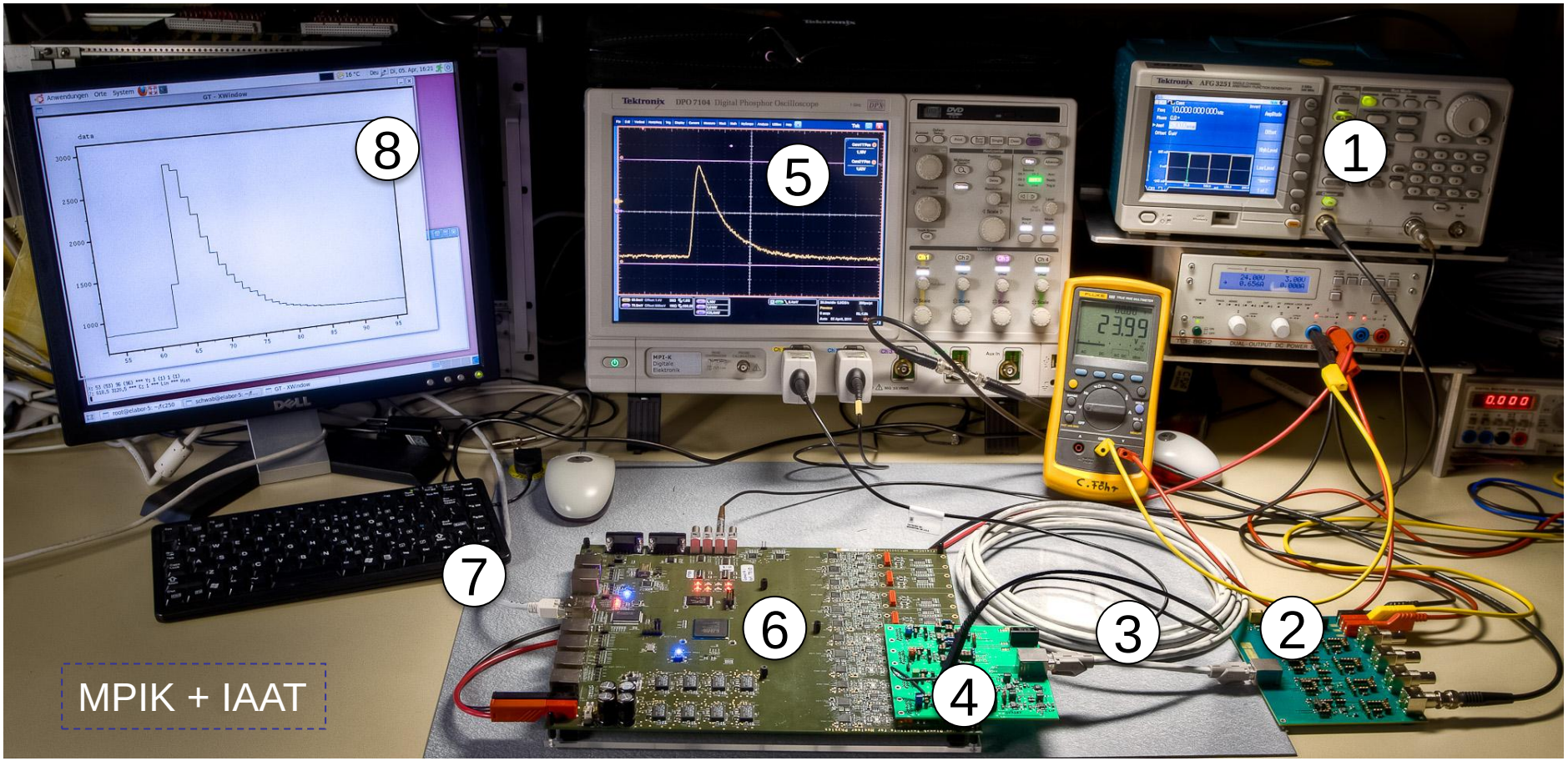
Camera Architecture

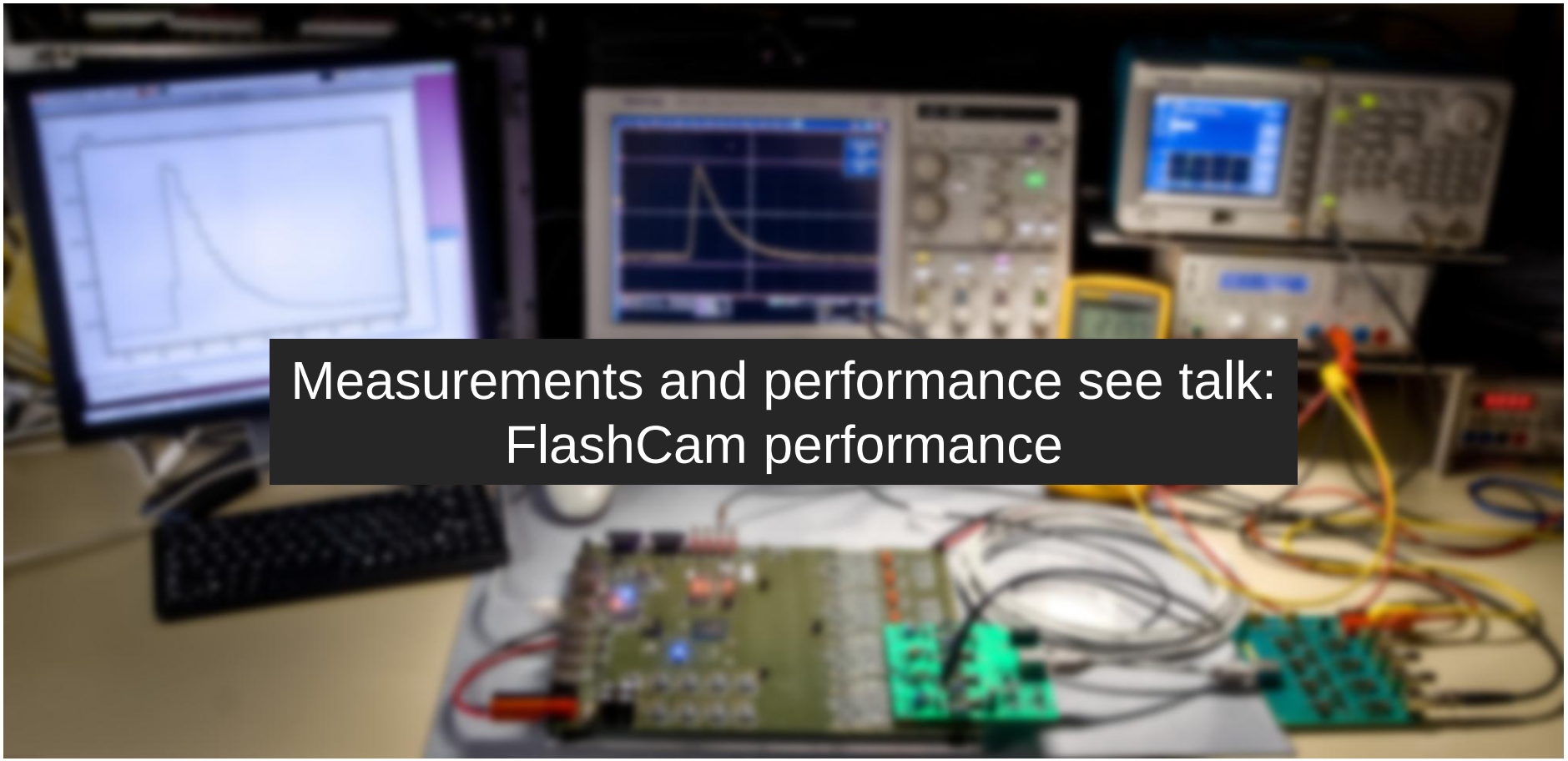


Parallel FADC Demo Board

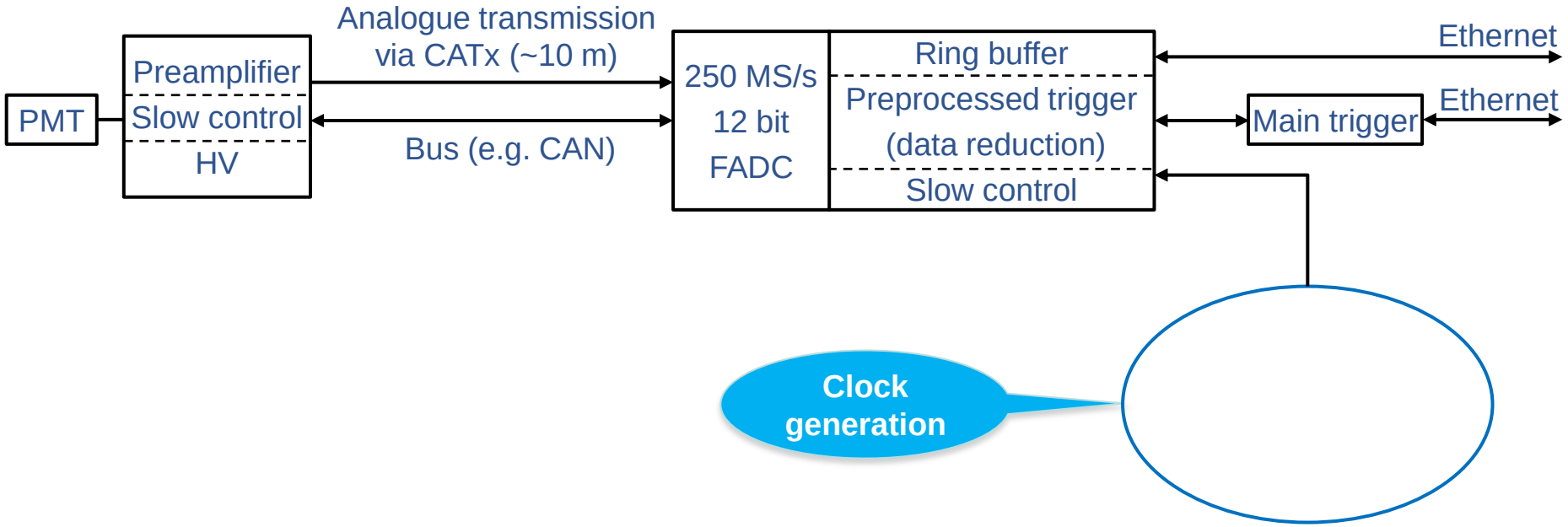


1 PMT pulse generator
2 Preamplifier board
3 Analogue signal transmission (CAT5)
4 ADC driver board
5 Analogue pulse before ADC
6 Demo board with 8 parallel FADCs and FPGA
7 Event transmission via LAN
8 Digitized pulse (4 ns / step)

Parallel FADC Demo Board



Camera Architecture

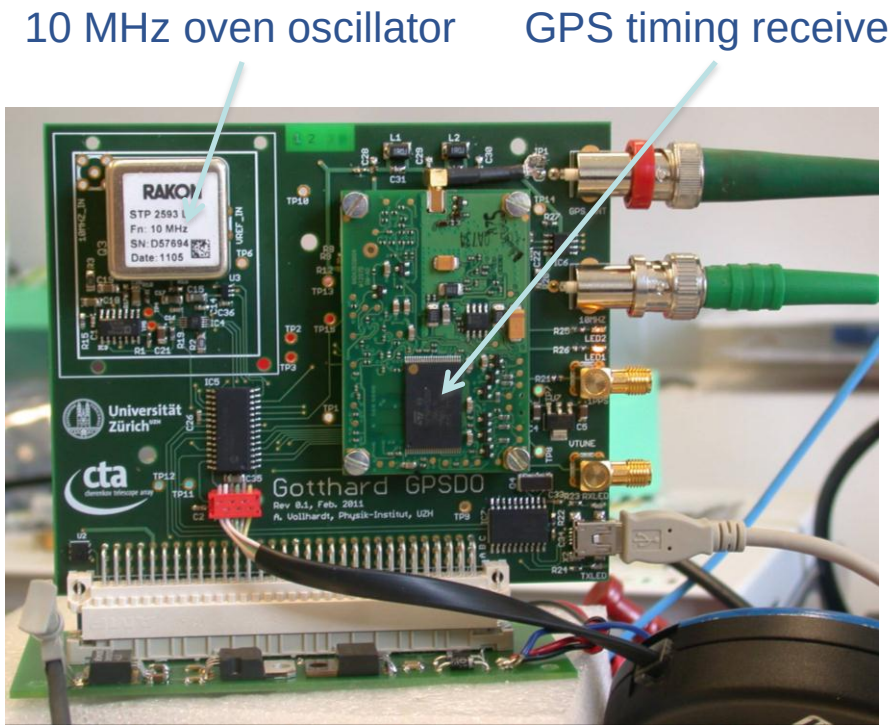


Clock Distribution

Clock generation:

- Single 10 MHz clock generation per telescope
  ⇨ eliminate need for array-wide clock distribution network
- Steered oscillator (PLL) using GPS 1pps signal compensating for oscillator aging and temperature effects
- Max. phase deviation to UTC ±15 ns
- Max. frequency deviation 1E-10
- Cost effective: < 500 € per unit

Testing in progress. More results in Toulouse.



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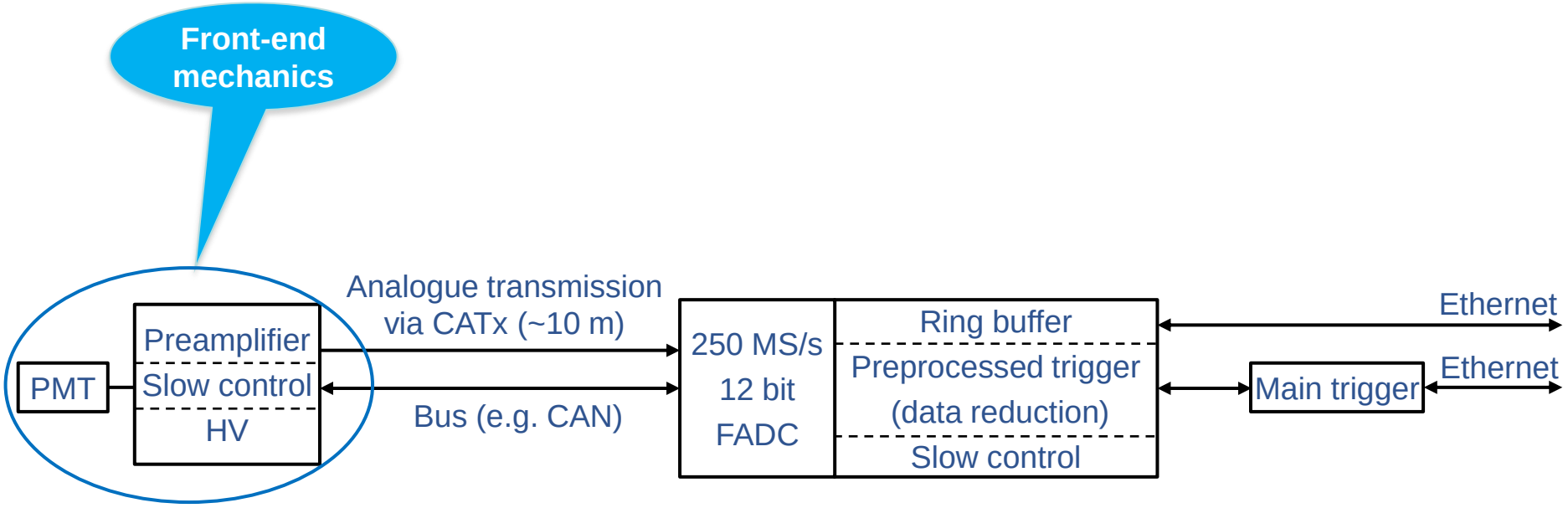
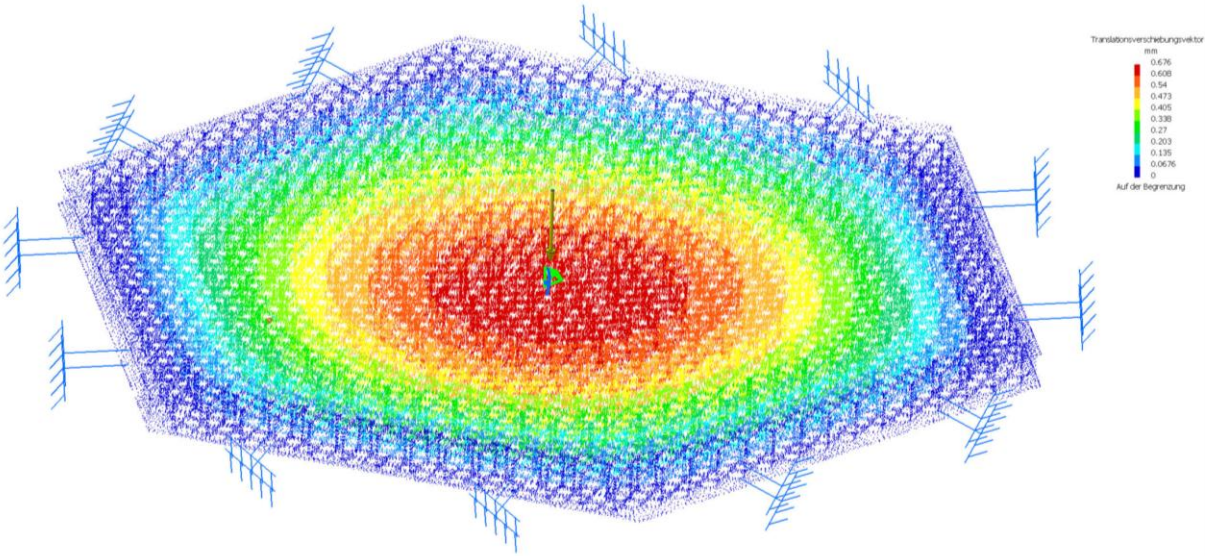
Camera Architecture



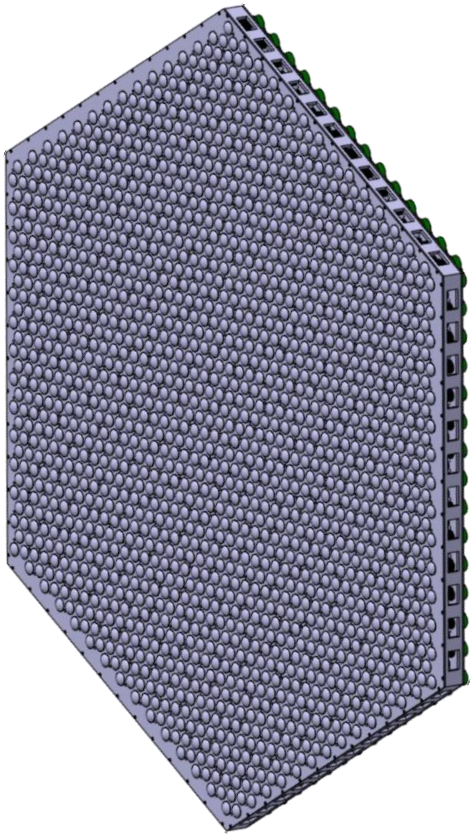
Front-end mechanics

An alternative to the drawer concept?

Structure weight: 81 kg
Flat to flat: 2170 mm
FEM calculation: 180 kg load at 90° → 0.68 mm sagging



Front view (without cones)



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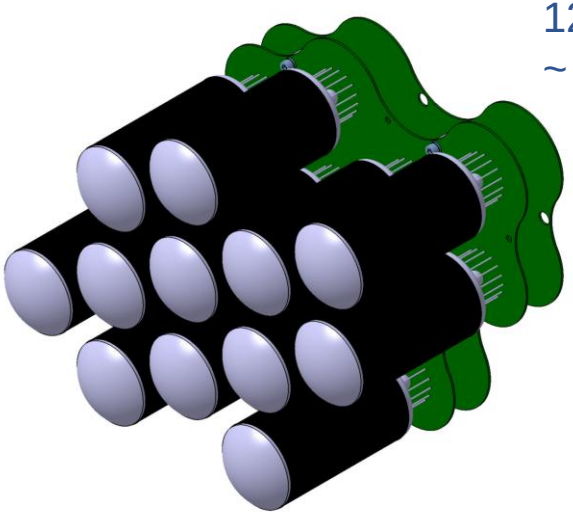
Front-end mechanics

12 PMTs module
~ 1.2 kg / module



147 modules, 1764 PMTs
~ 180 kg (incl. electronics)

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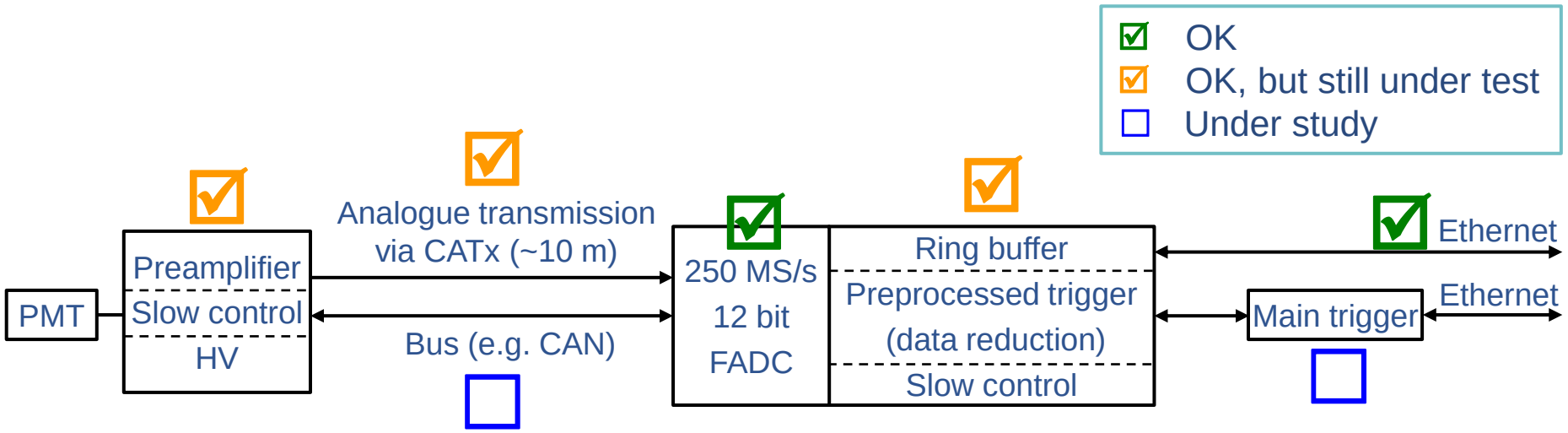
Summary and Outlook

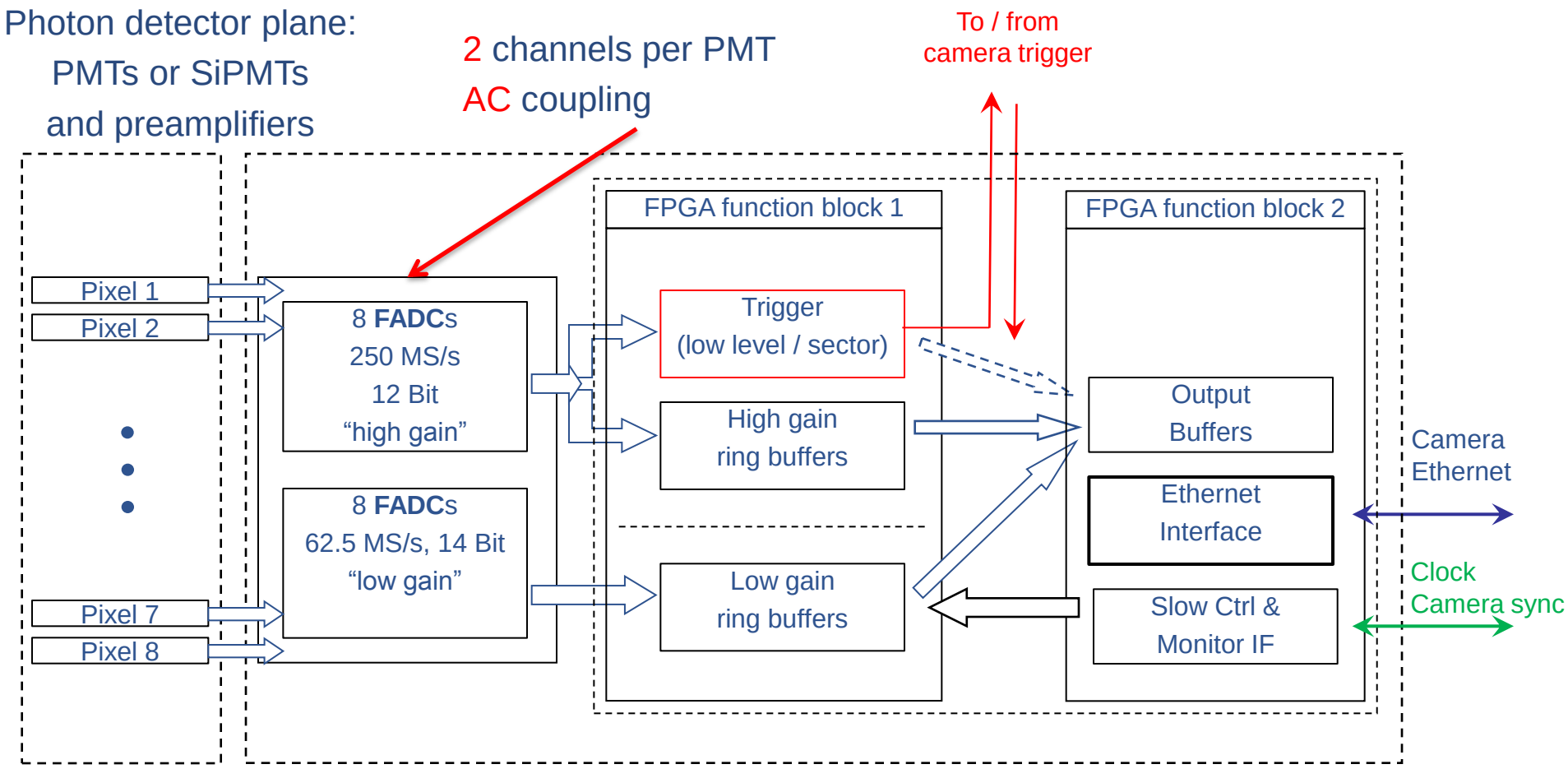


Outlook

- 24 parallel FADCs demo board planned
- Extensive measurements with serial FADCs demo board
- Test and implementation of main trigger algorithms
- Further development and implementation of slow control concept
- Full camera electronics implementation (PDP module, crates etc.)

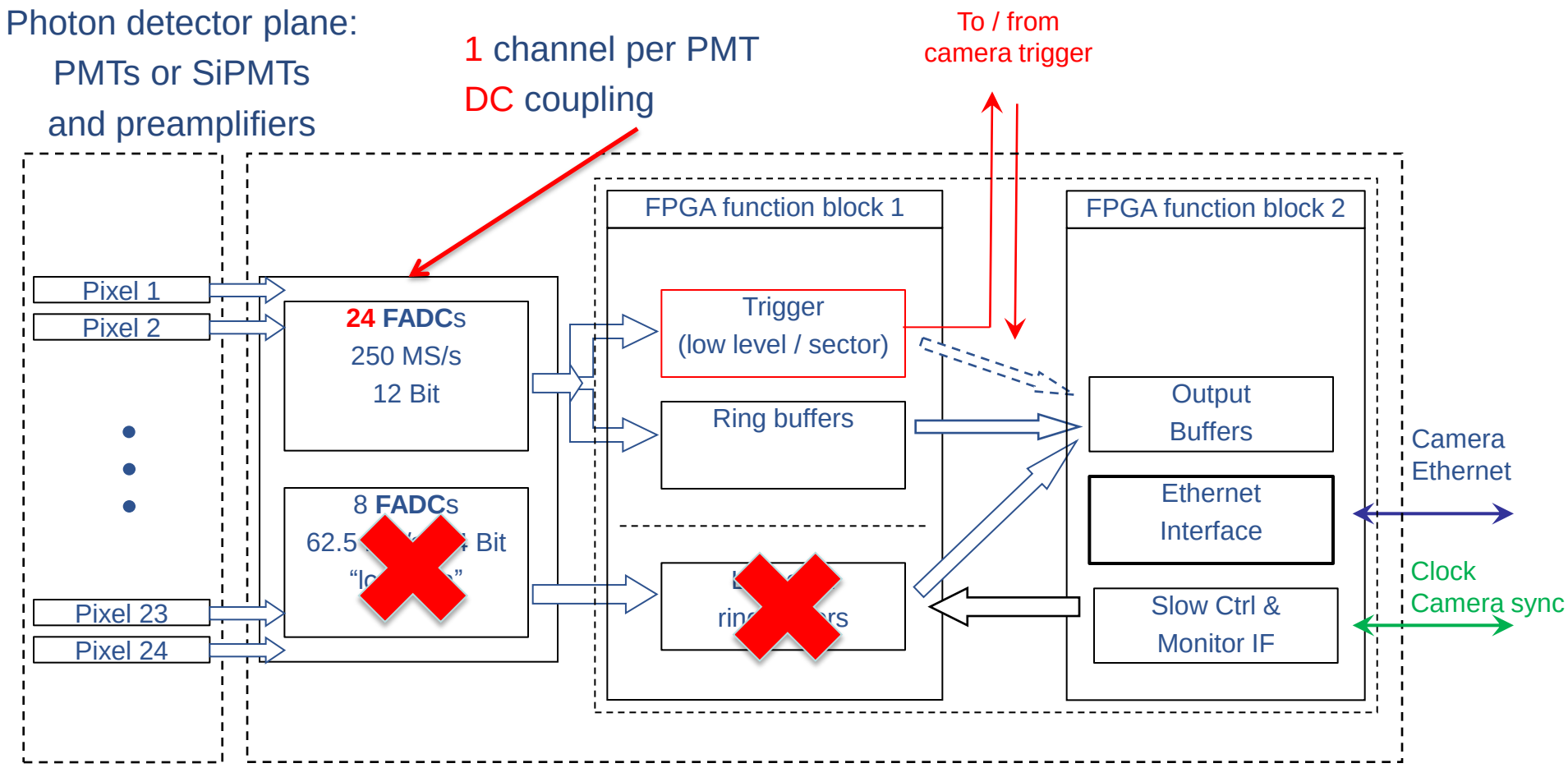
Backup

FADC-based front-end: Old topology



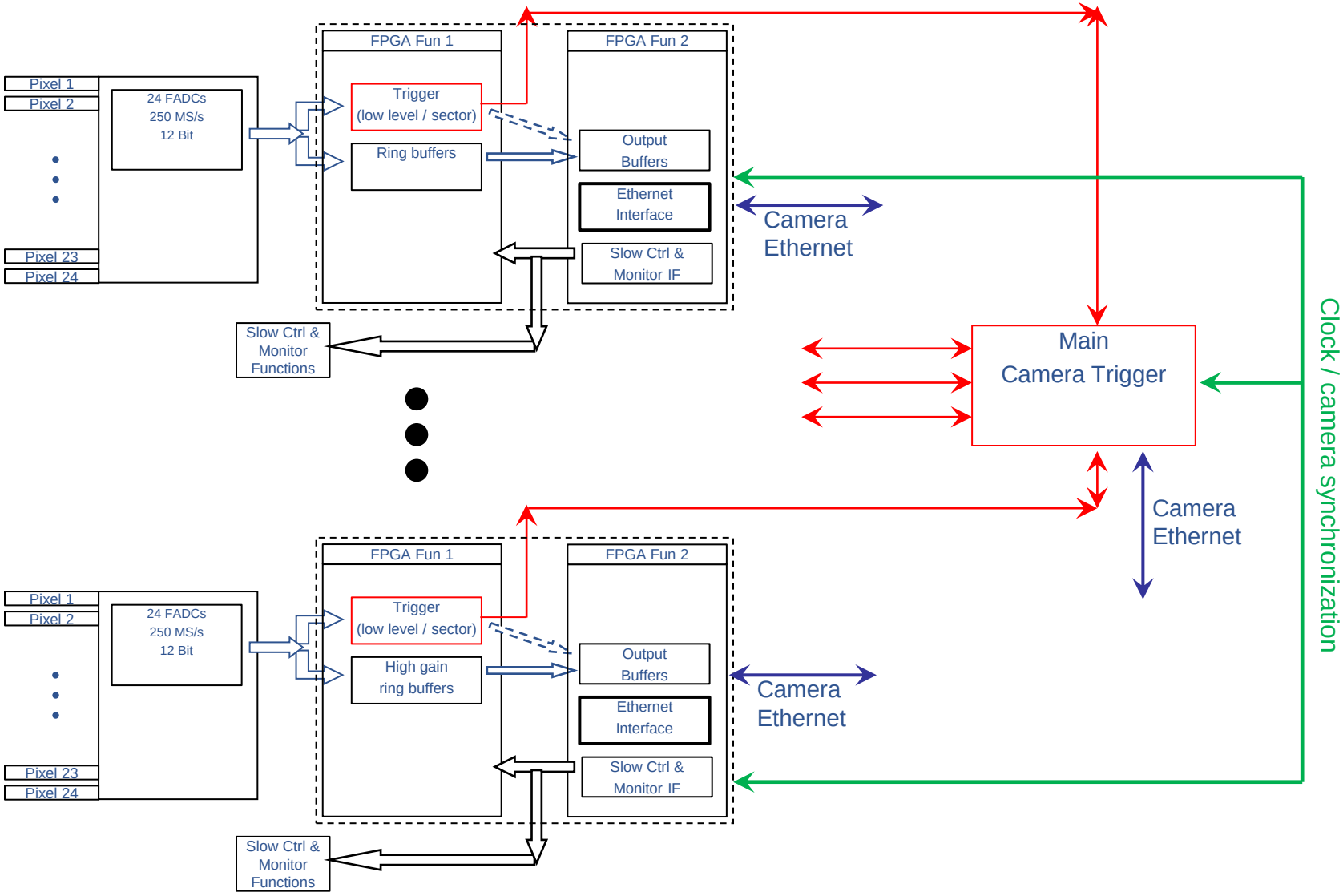
FADC / FPGA based trigger and readout

FADC-based front-end: New topology

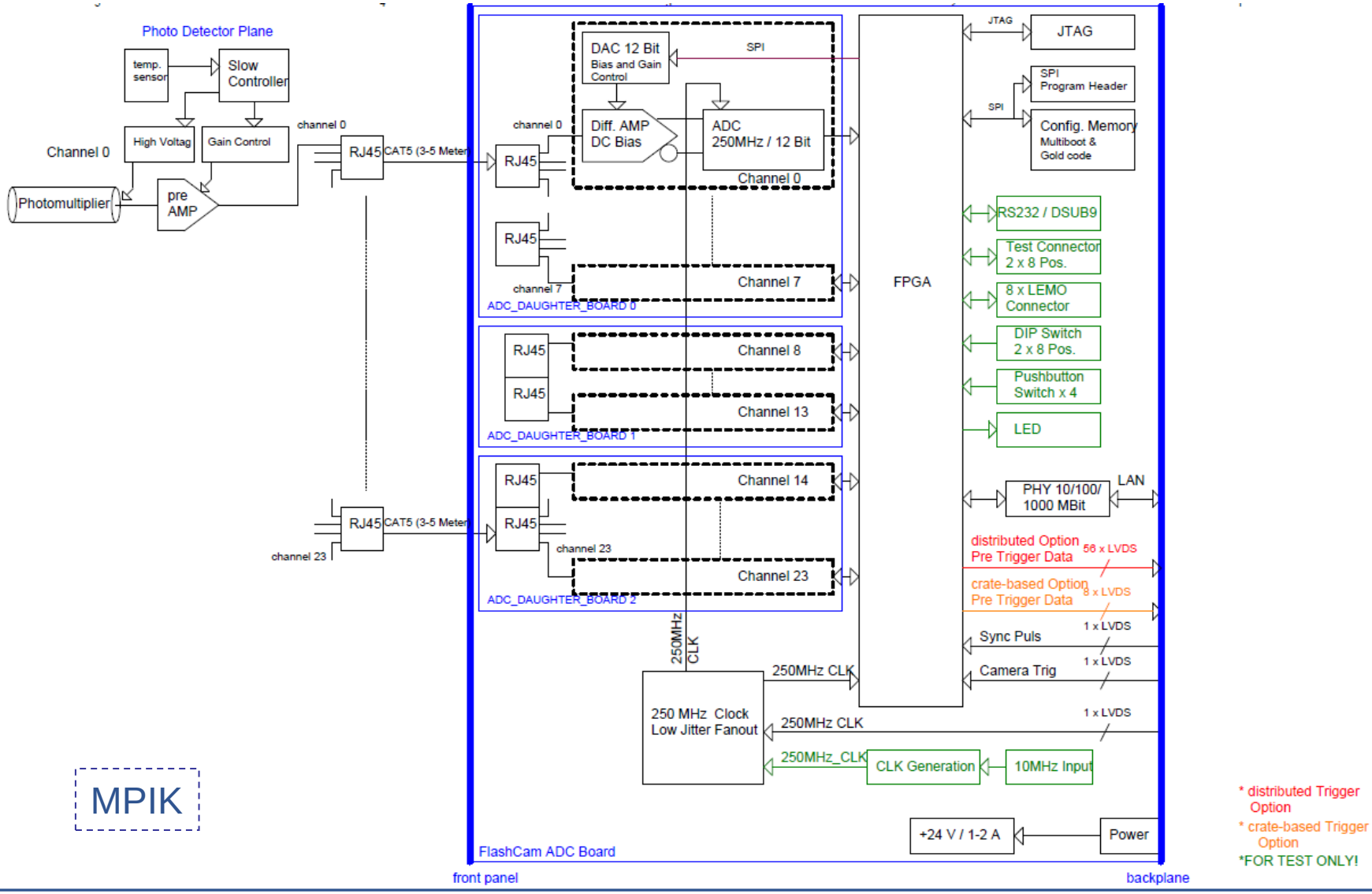


FADC / FPGA based trigger and readout

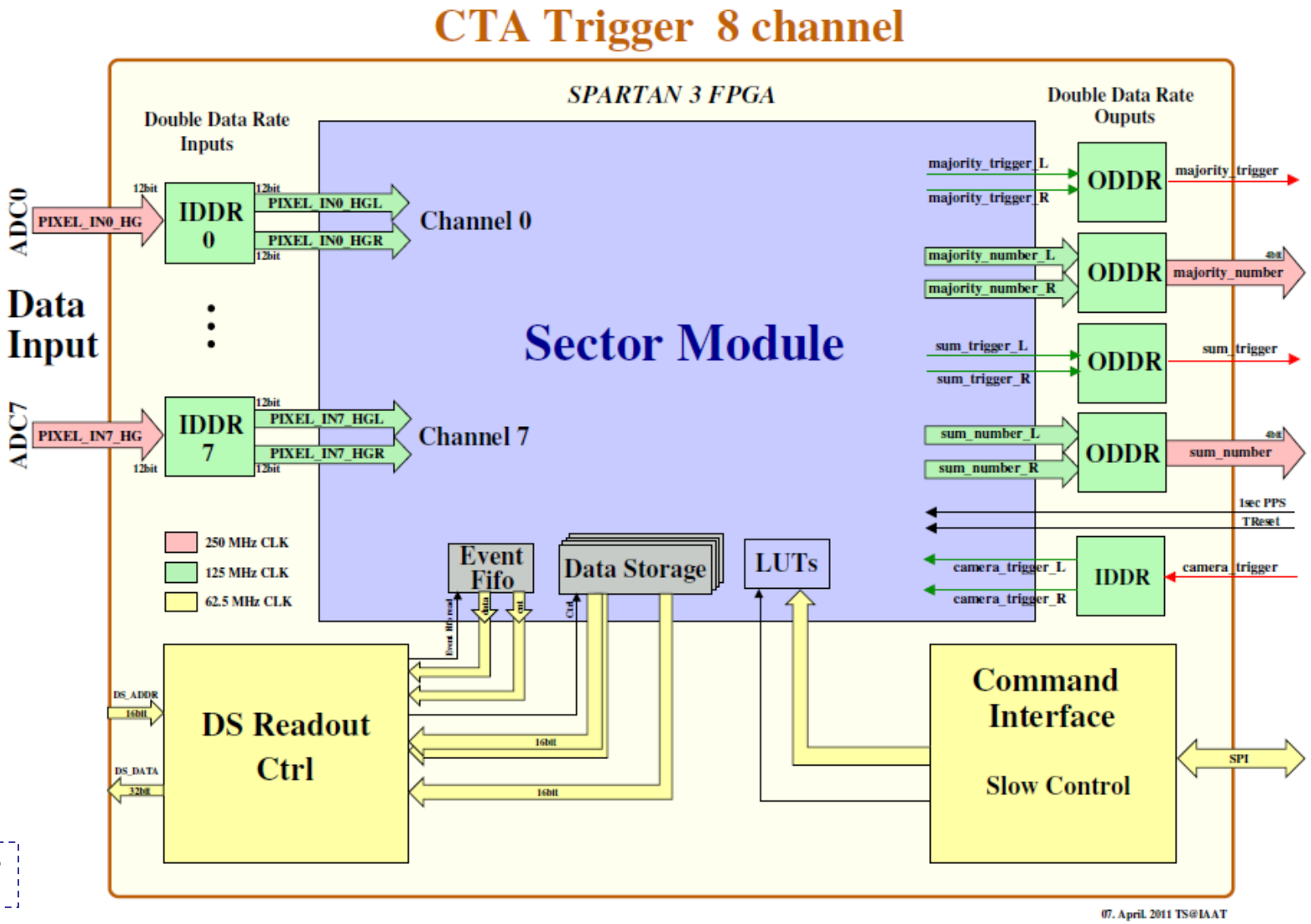
So the overall Camera Architecture looks like



FlashCam blockdiagram



Sector trigger blockdiagram



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Saturation preamplifier

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Overdrive (AD8000 documentation)

Overdrive caused by too large input signal

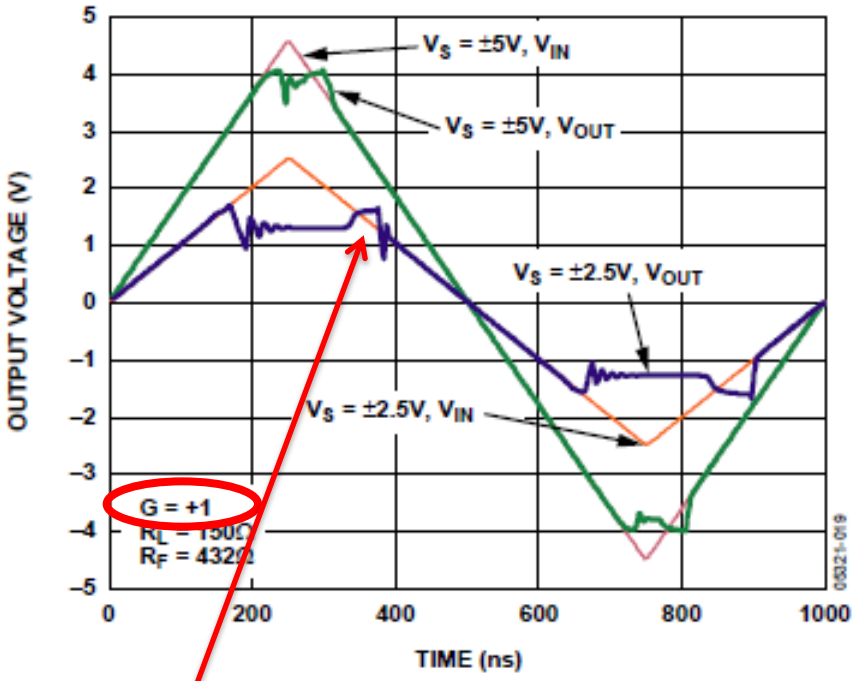


Figure 38. Input Overdrive

Ringing can be avoided with clipping diodes.

Overdrive caused by amplification

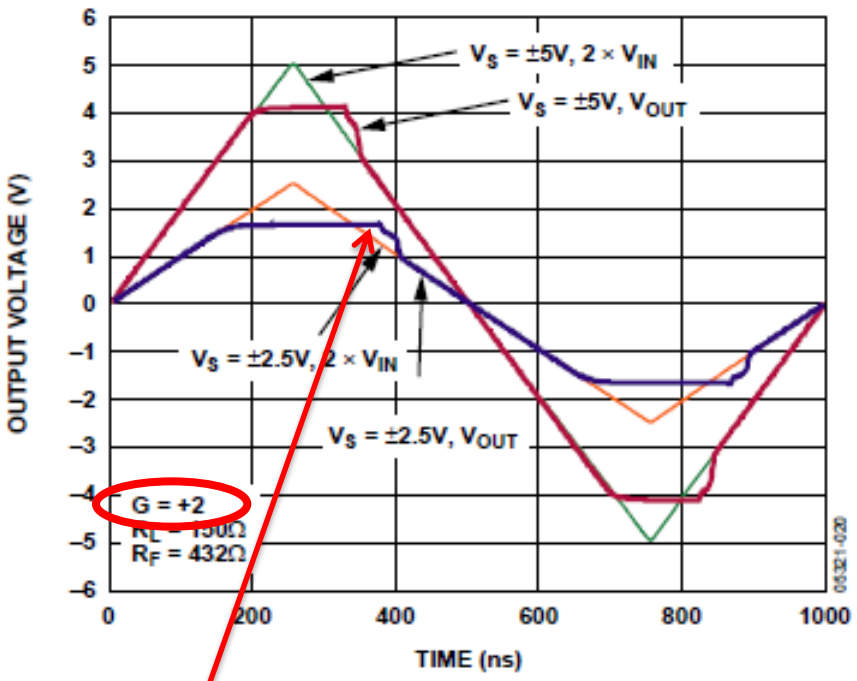
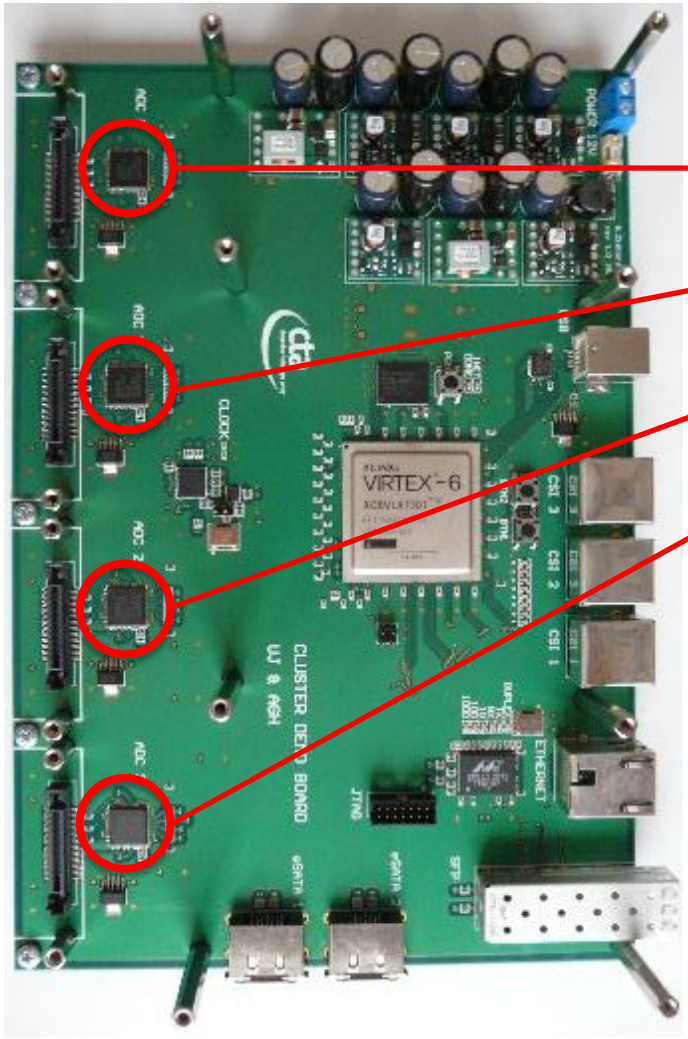
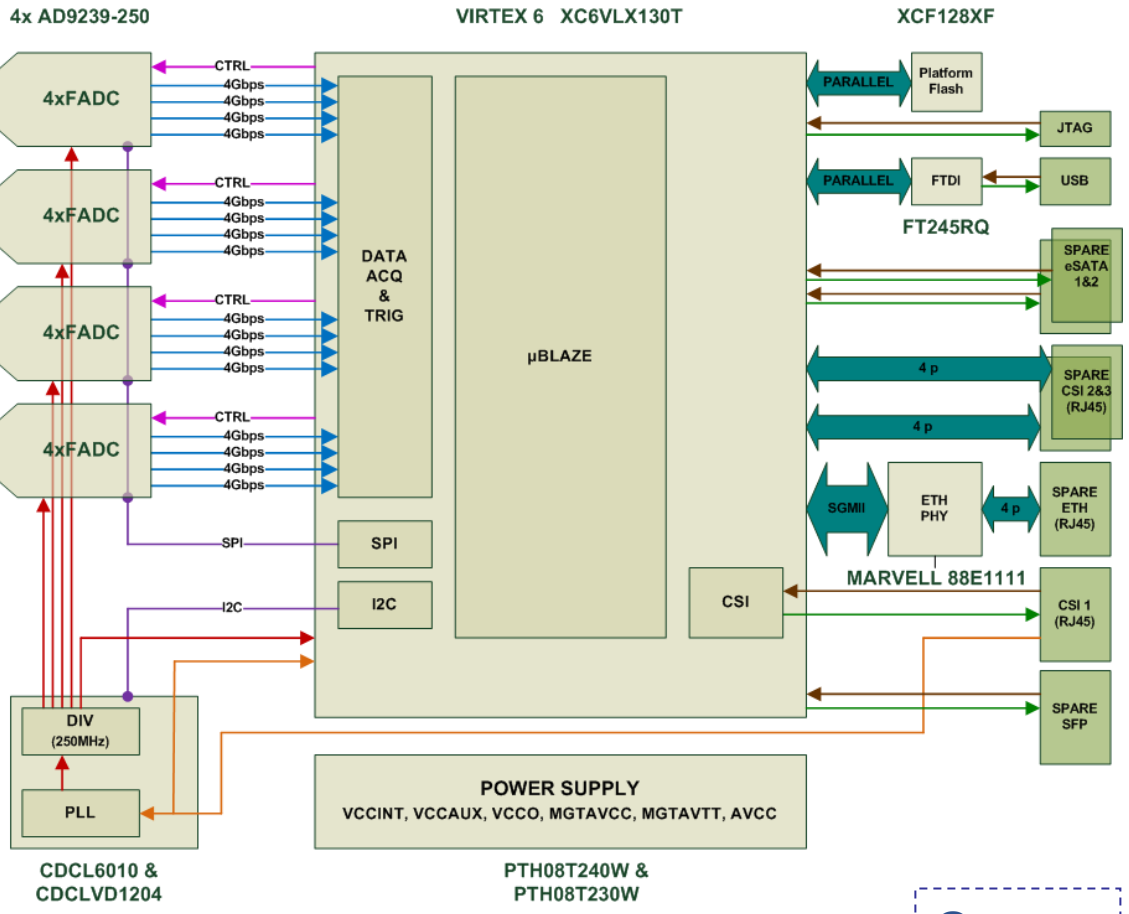


Figure 39. Output Overdrive

Saturation of output signal with defined recovery time.

Serial FADC FlashCam Demo Board





Cracow

Ethernet-Based Readout

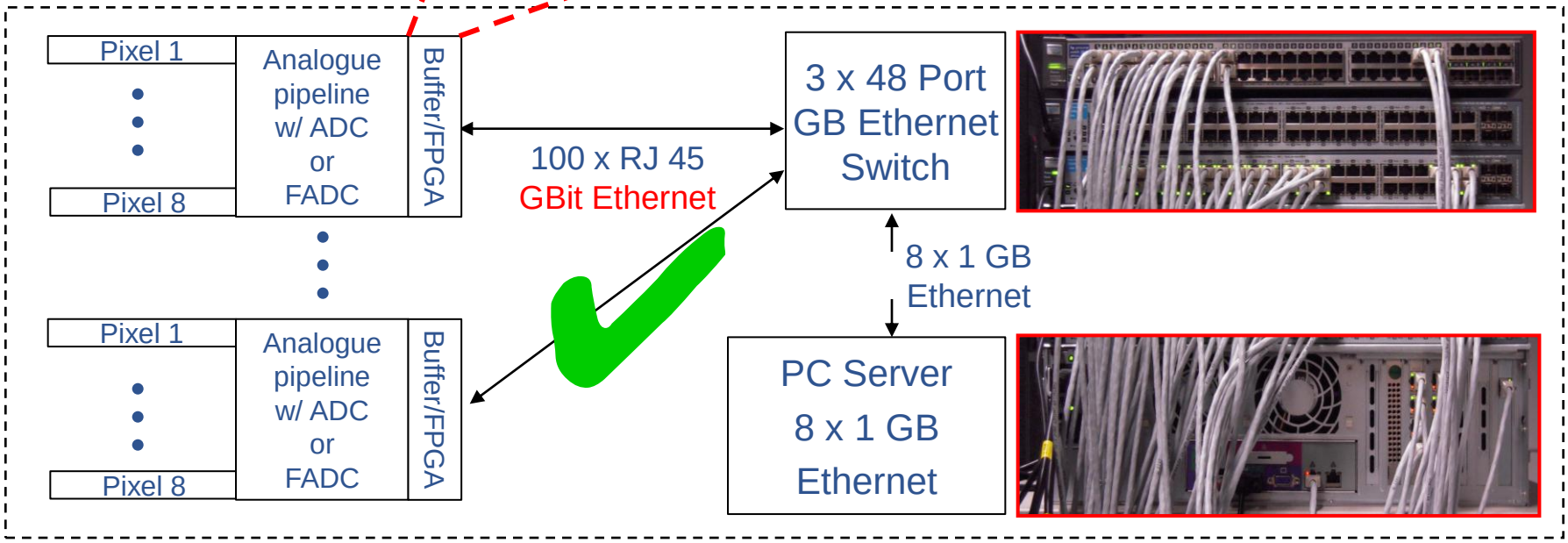
Design parameters:
- readout window: 30 nsec
- Assume 1.5 Byte / pix / sample
- 2000 pixels
- ≤10 kHz camera triggers

Dead time free

Sampling Frequency	Samples /event/pix	Data Rate
250 MS/s	10	~400 MByte / s
1 GS/s (hi, lo)	60	1.8 GByte / s
2 GS/s (hi, lo)	120	3.6 GByte / s

FPGA as Eth sender

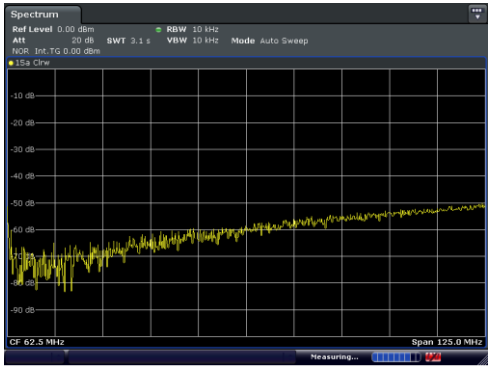
Tested: 700 MByte/sec (loss free)



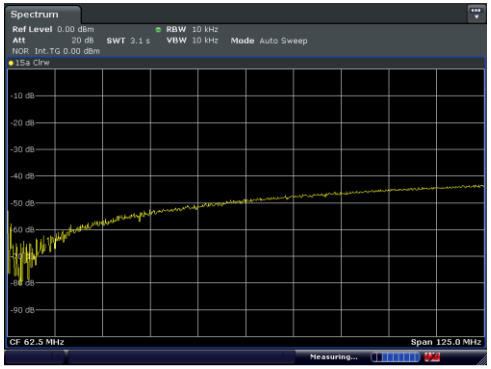
CAT 5 for Analogue Signal Transmission

No plug inserted

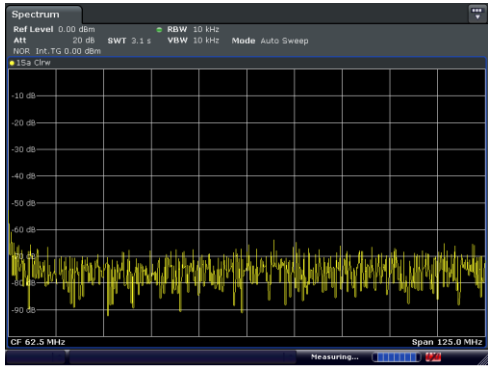
CH1 to CH2



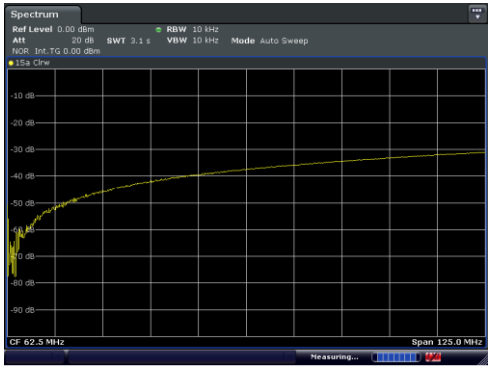
CH1 to CH3



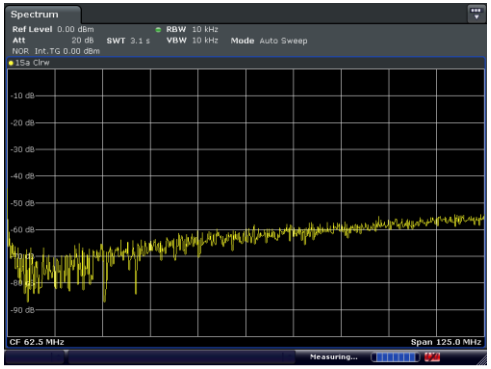
CH1 to CH4



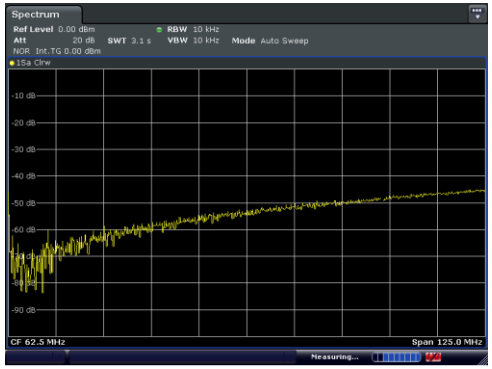
CH2 to CH3 !!!



CH2 to CH4



CH3 to CH4

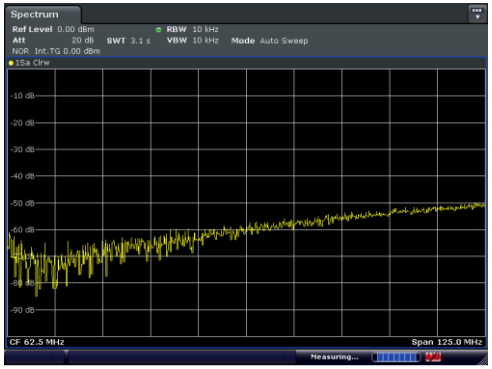


Cracow

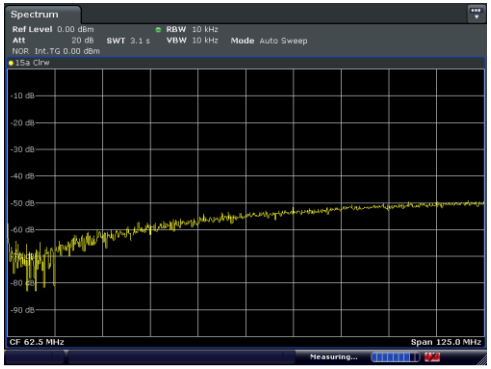
CAT 5 for Analogue Signal Transmission

Naked plug inserted (no cable)

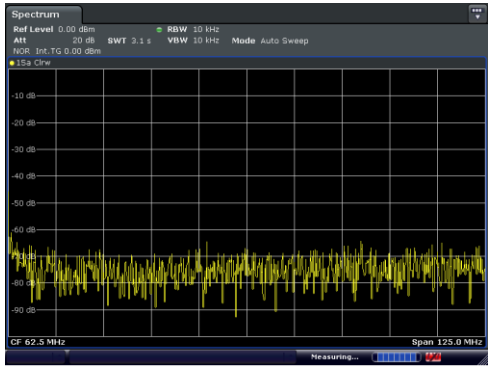
CH1 to CH2



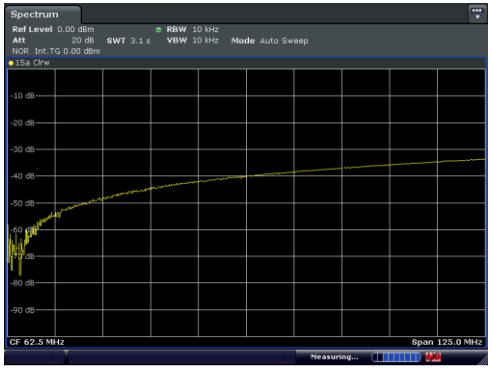
CH1 to CH3



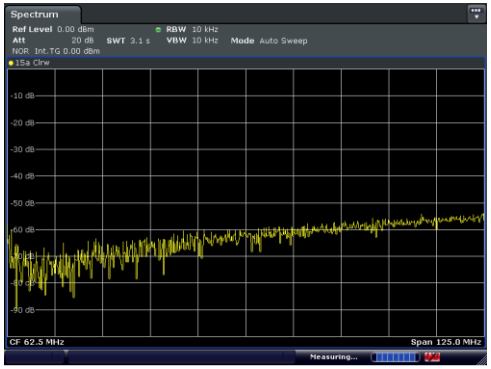
CH1 to CH4



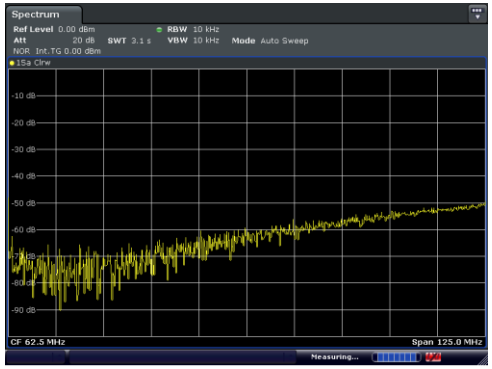
CH2 to CH3 !!!



CH2 to CH4

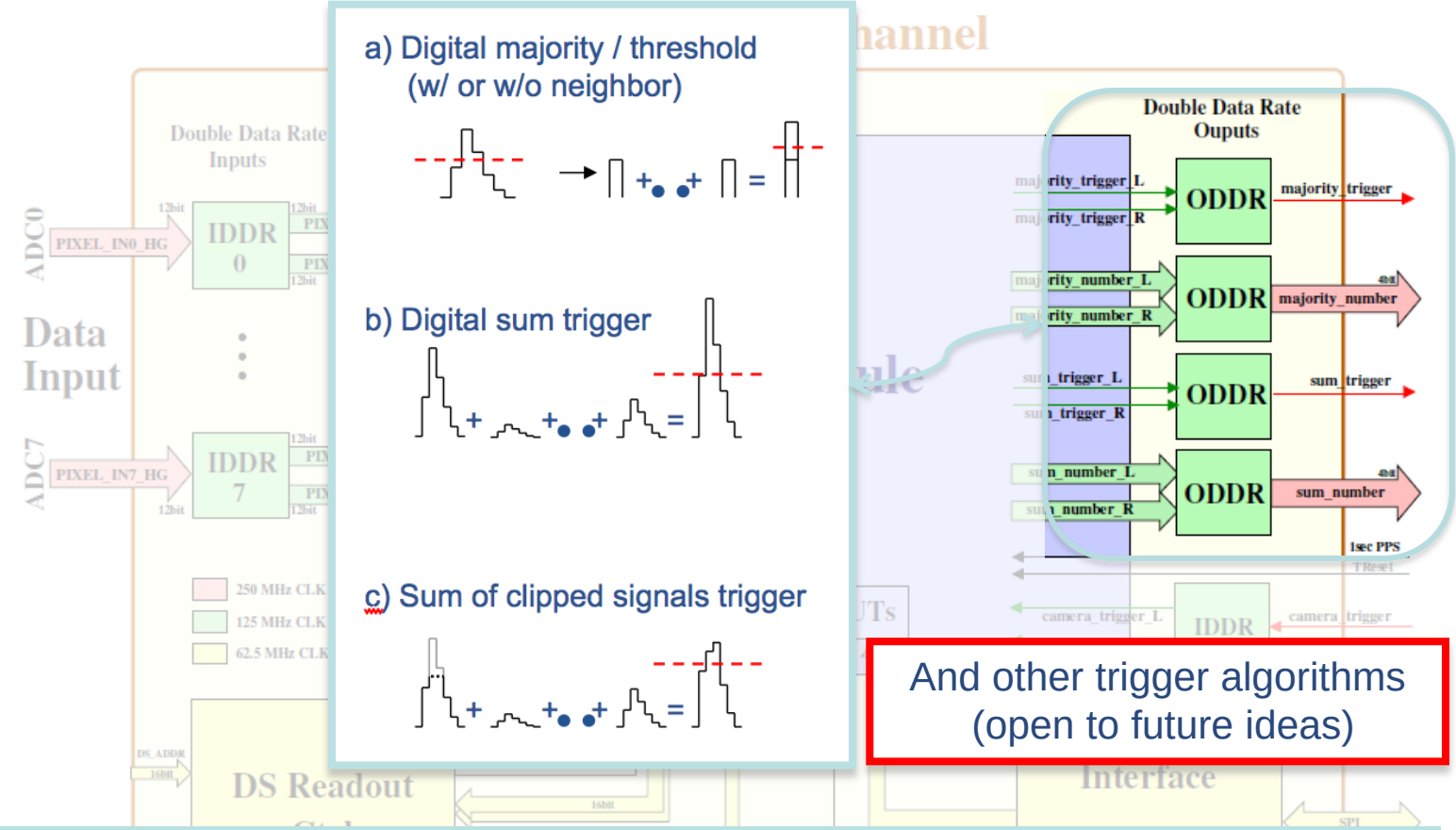


CH3 to CH4



Cracow

Sector FPGA Layout



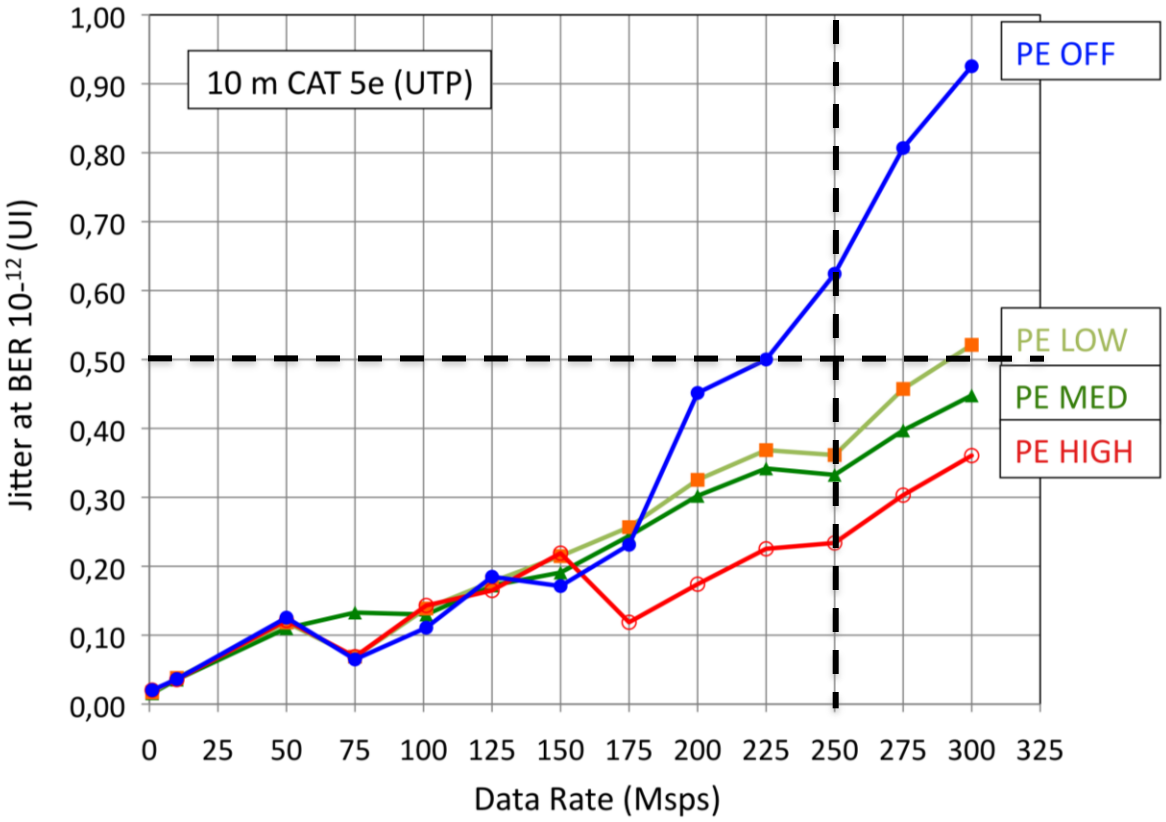
Flexible trigger system, no separate hardware needed.

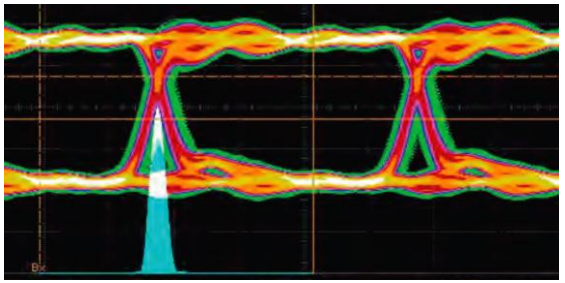
Clipping can be switched on to suppress impact of afterpulsing.

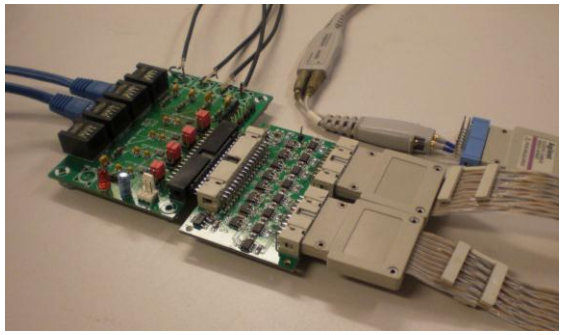
IAAT

Clock and Trigger Distribution: Parallel

Leeds/Leicester







➔ CAT cables well suited for digital signal transmission at ~ 250 MS/s